
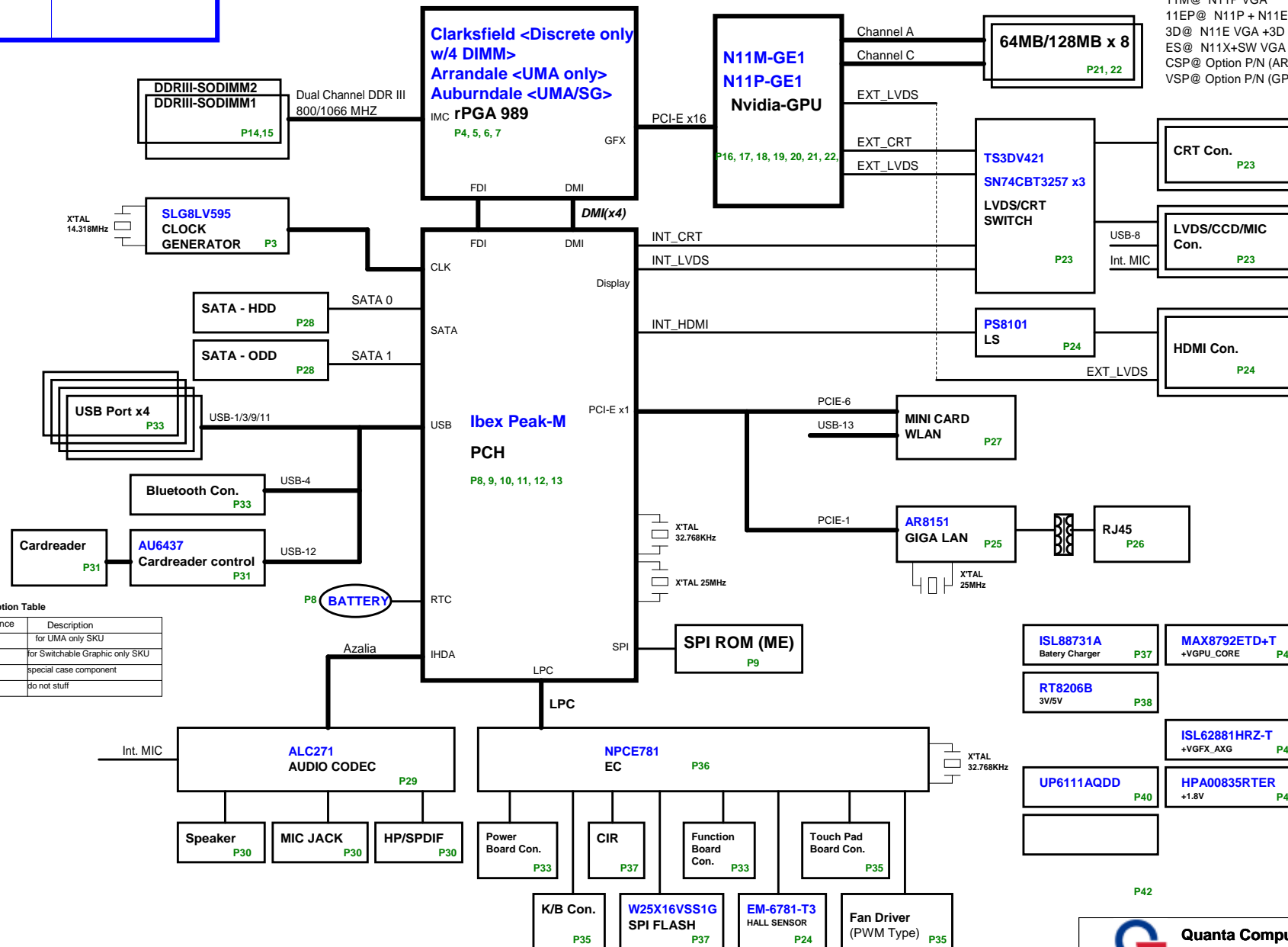


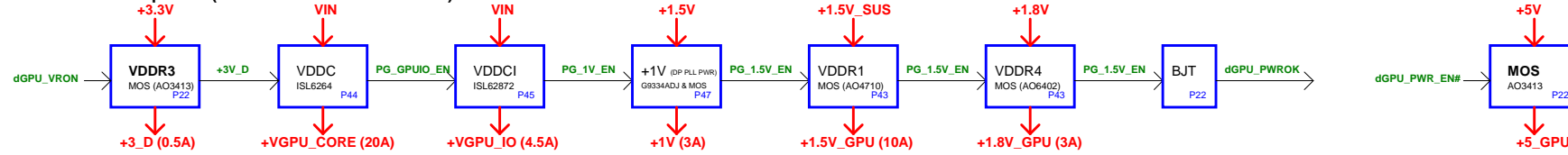
## ZR7 SYSTEM BLOCK DIAGRAM

IV@ INT VGA  
EV@ DISCRETE  
SW@ SW VGA  
11P@ N11P VGA  
11M@ N11P VGA  
11EP@ N11P + N11E VGA  
3D@ N11E VGA +3D  
ES@ N11X+SW VGA  
CSP@ Option P/N (ARD&R D)  
VSP@ Option P/N (GPU/ VRAM)

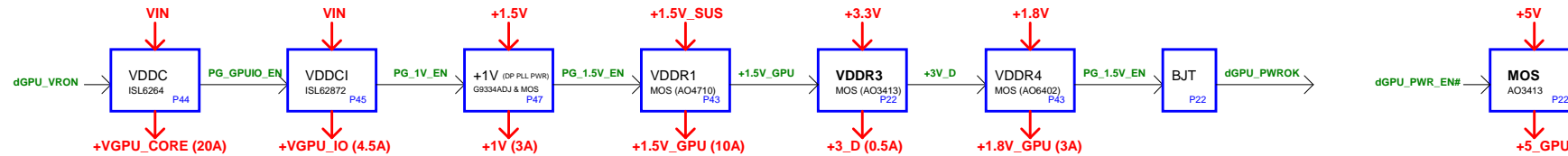
 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		Rev
Size	Document Number	3E
<b>Block Diagram</b>		
Date:	Monday, February 22, 2010	Sheet 1 of 49



### GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



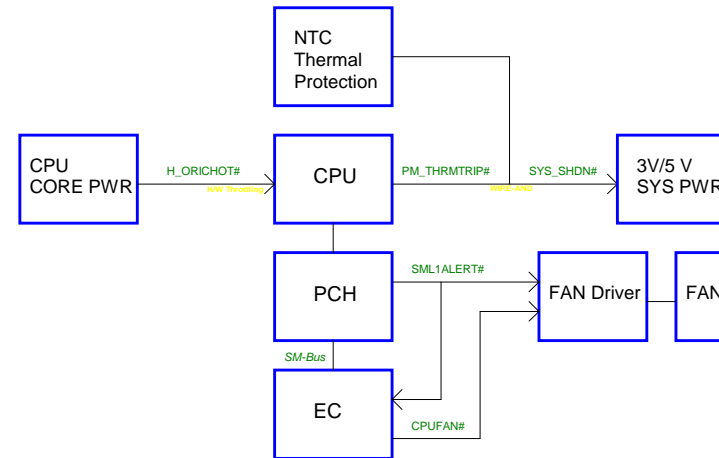
### GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



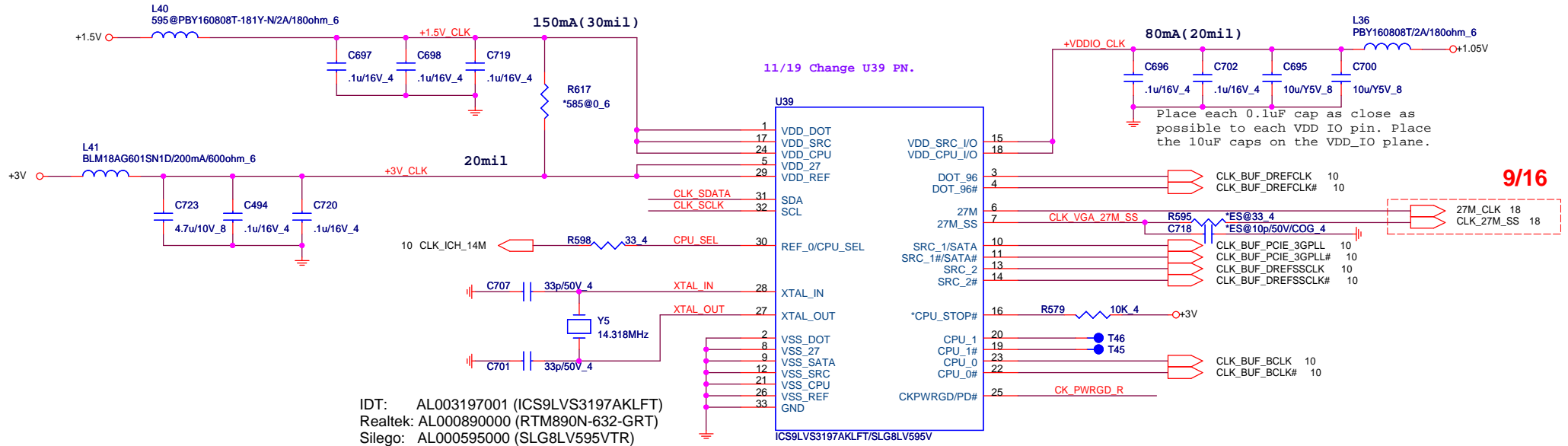
### Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

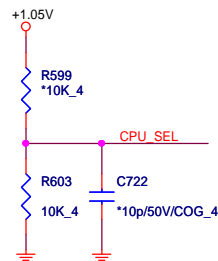
### Thermal Follow Chart



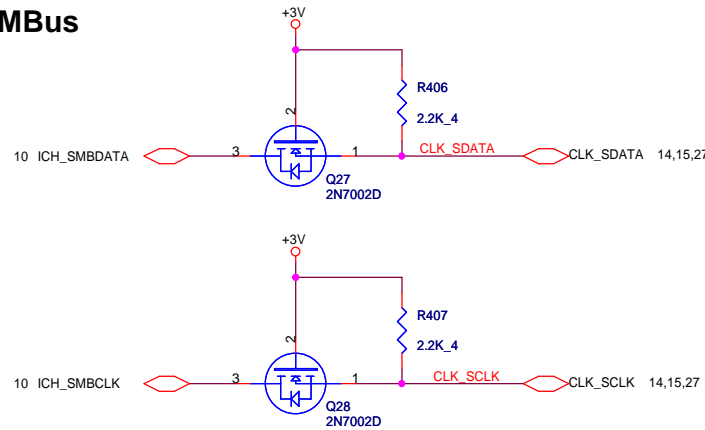
## CLK GEN.



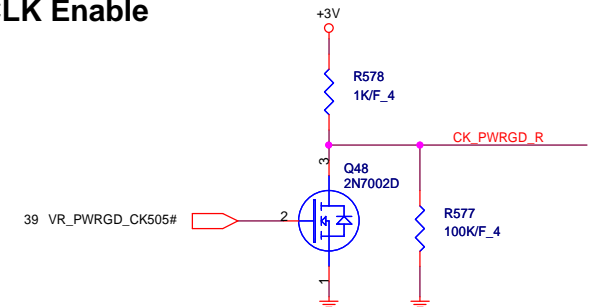
## CPU\_CLK select



## SMBus

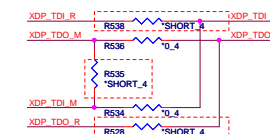
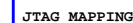



## CLK Enable



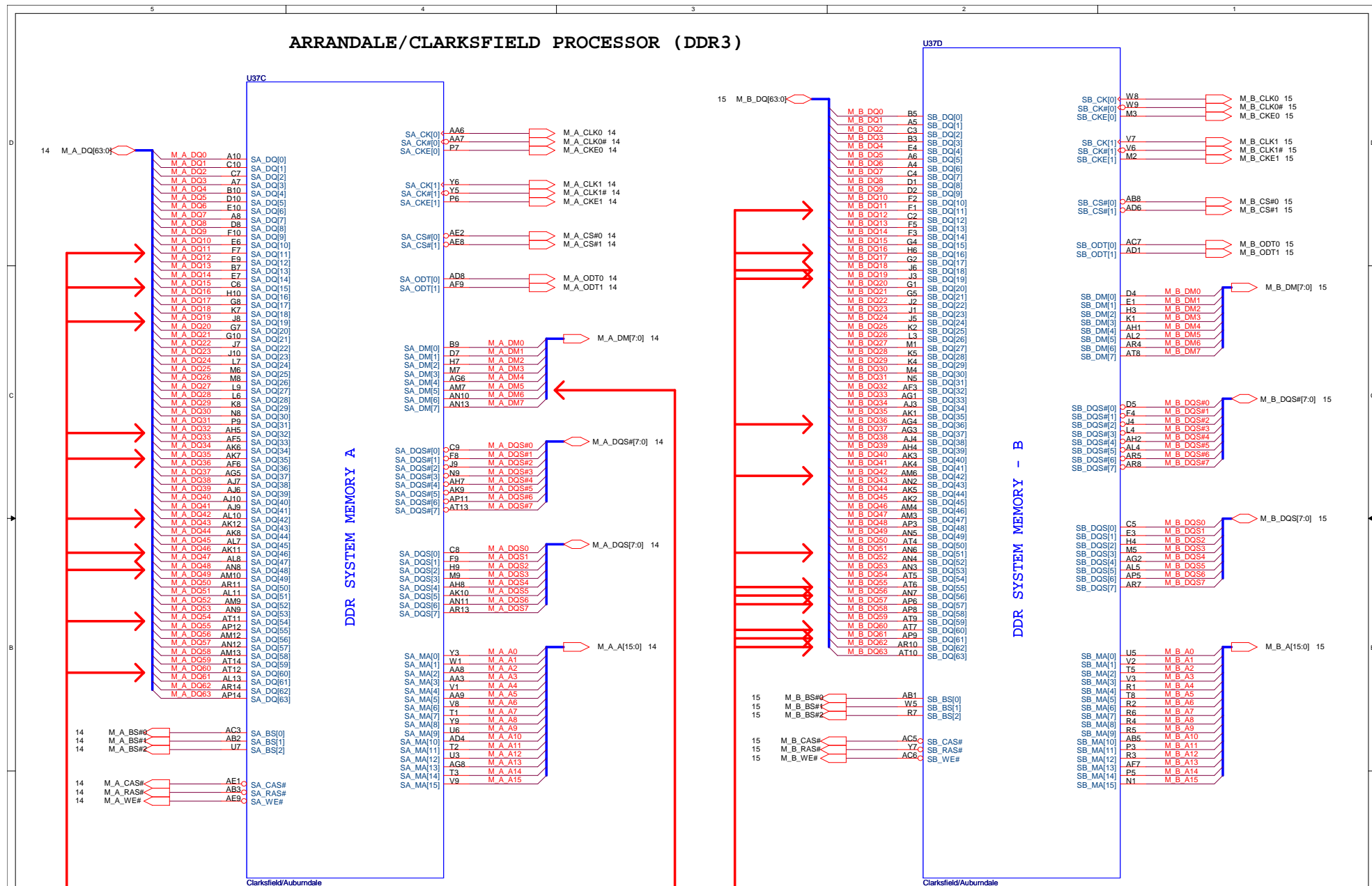
**Quanta Computer Inc.**  
**PROJECT : ZR7**

Size	Document Number	Rev
	<b>Clock Generator</b>	3B
Date:	Monday, February 22, 2010	Sheet 3 of 49



 **Quanta Computer Inc.**  
PROJECT : ZR7

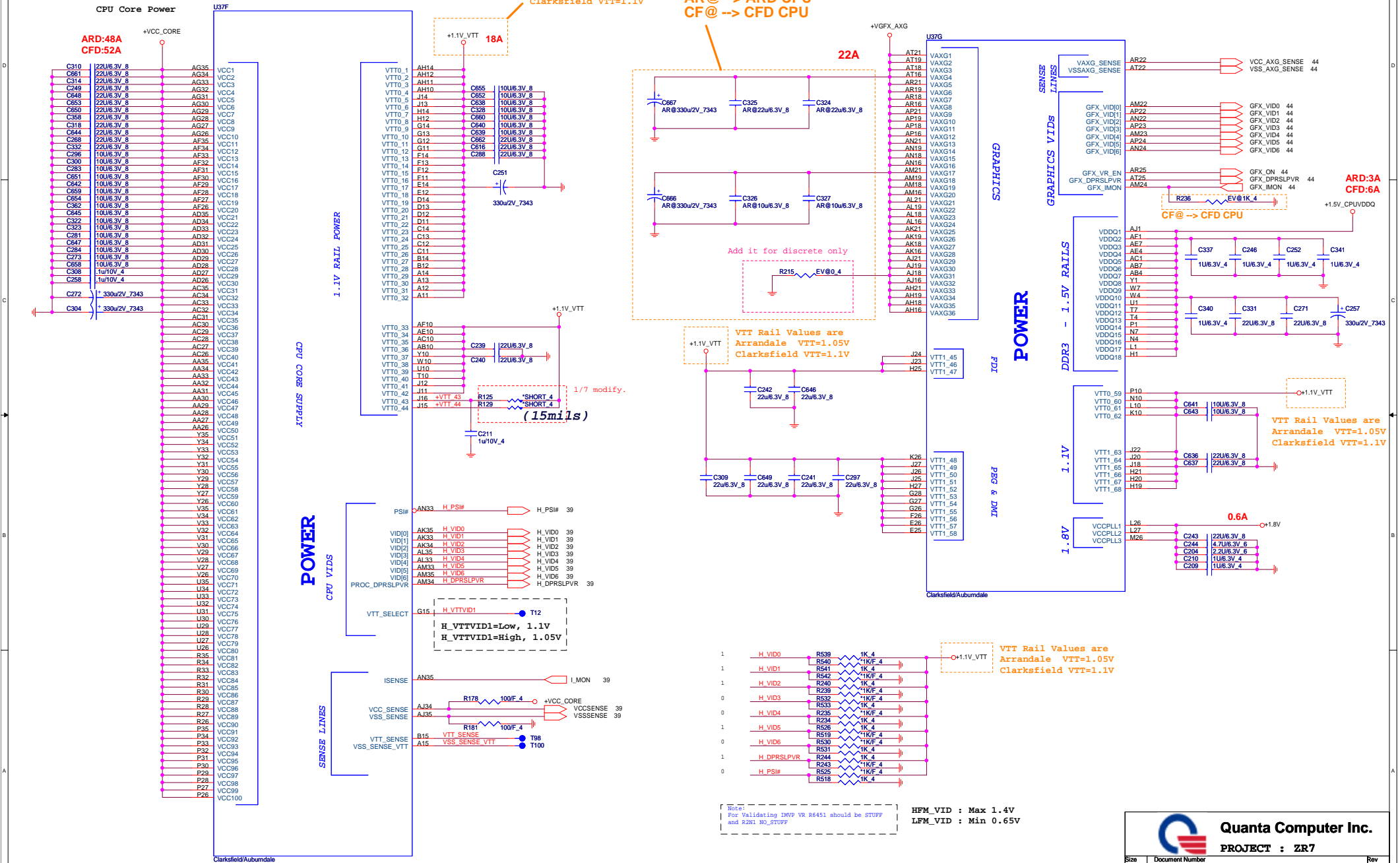
# ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



## ARRANDALE/CLARKSFIELD PROCESSOR (POWER)

**CF@ --> CFD CPU**

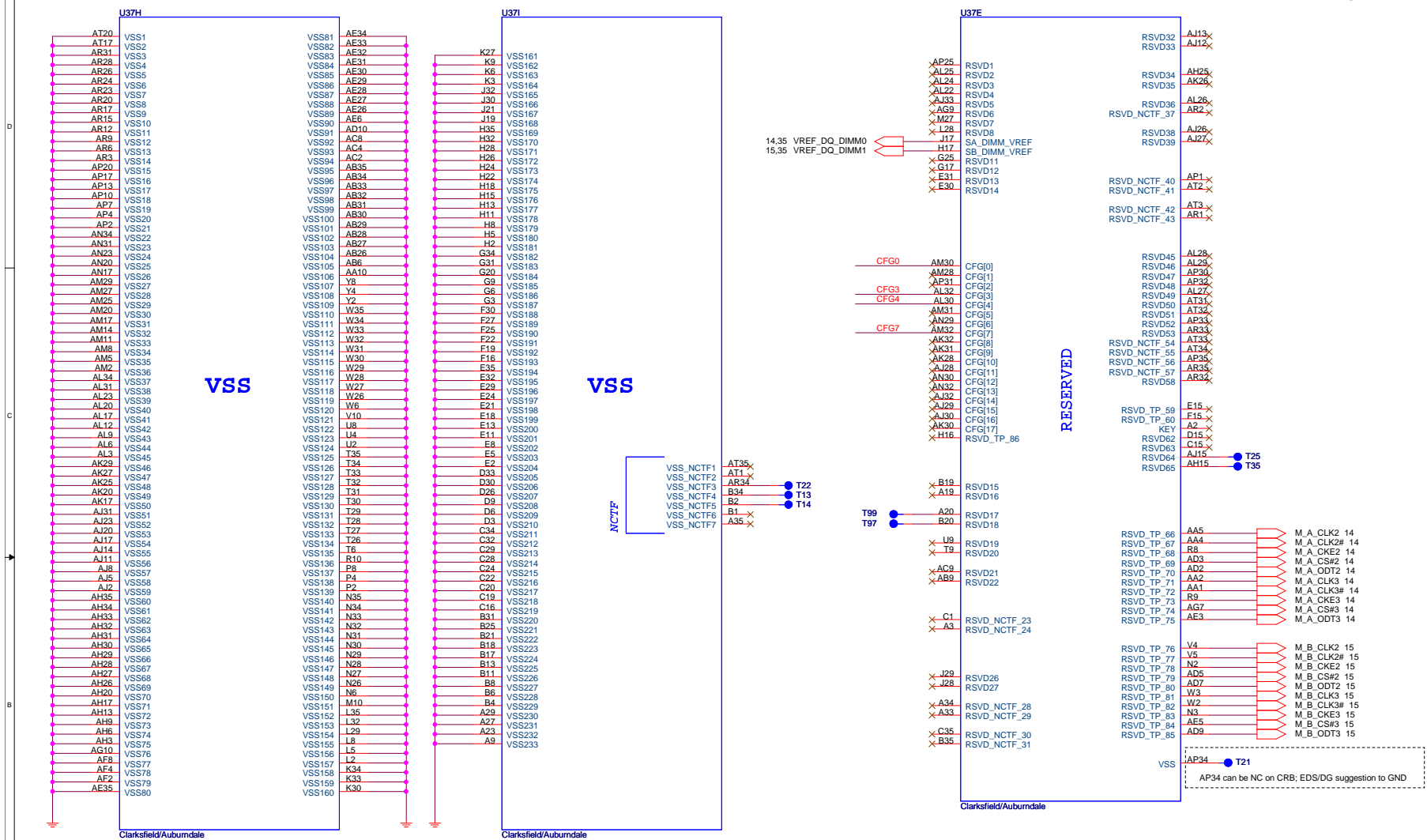
## ARRANDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)





# ARRANDALE/CLARKSFIELD PROCESSOR (GND)

# ARRANDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)

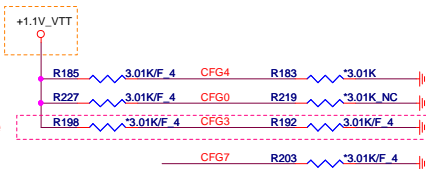


## Processor Strapping

	1	0	DEFAULT
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.			

VTT Rail Values are  
Arrandale VTT=1.05V  
Clarksville VTT=1.1V

Use reverse type



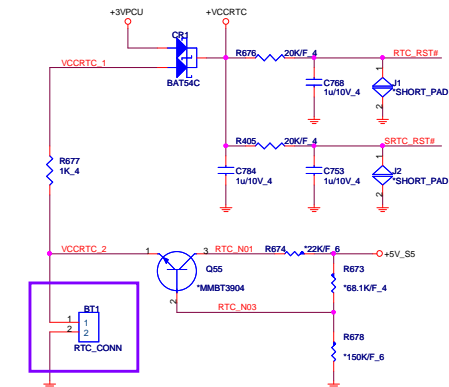
**Quanta Computer Inc.**  
PROJECT : ZR7

Size	Document Number	Rev
	ARRANDALE/CLARKSFIELD 4/4	3B
Date:	Monday, February 22, 2010	Sheet 7 of 49



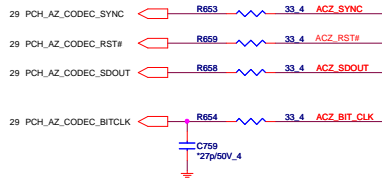


## RTC Circuitry



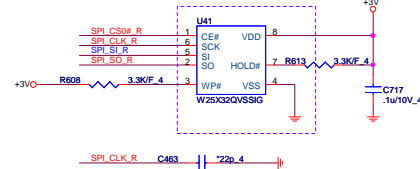
1/7 Change P/N by ME.

## HDA Bus

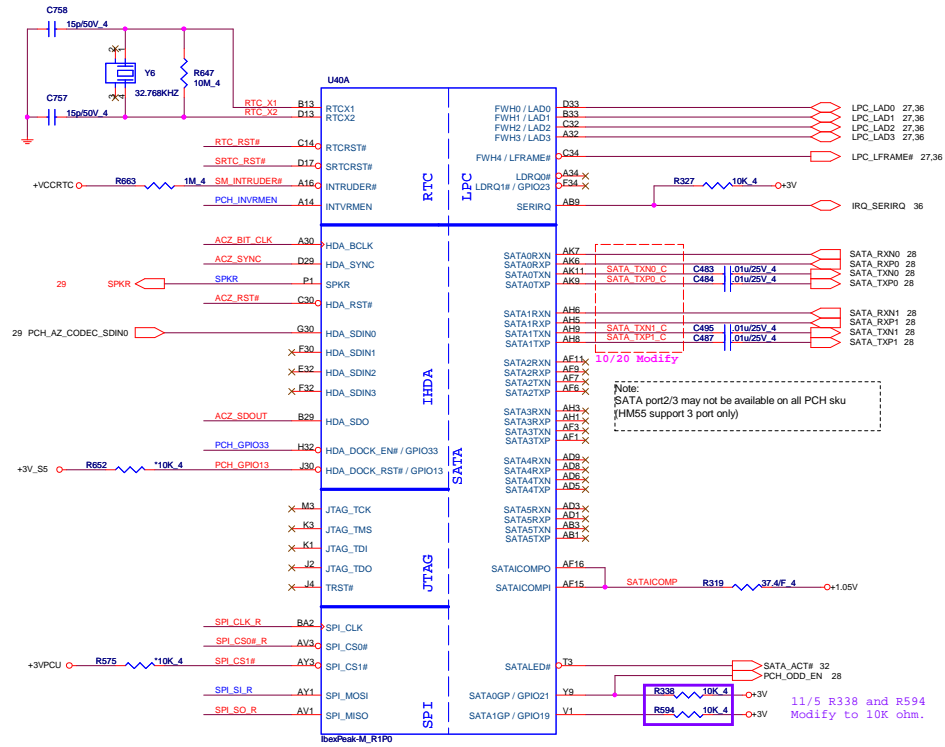


## PCH SPI

10/29 Modify P/N to 2M  
12/7 Modify P/N to 4M



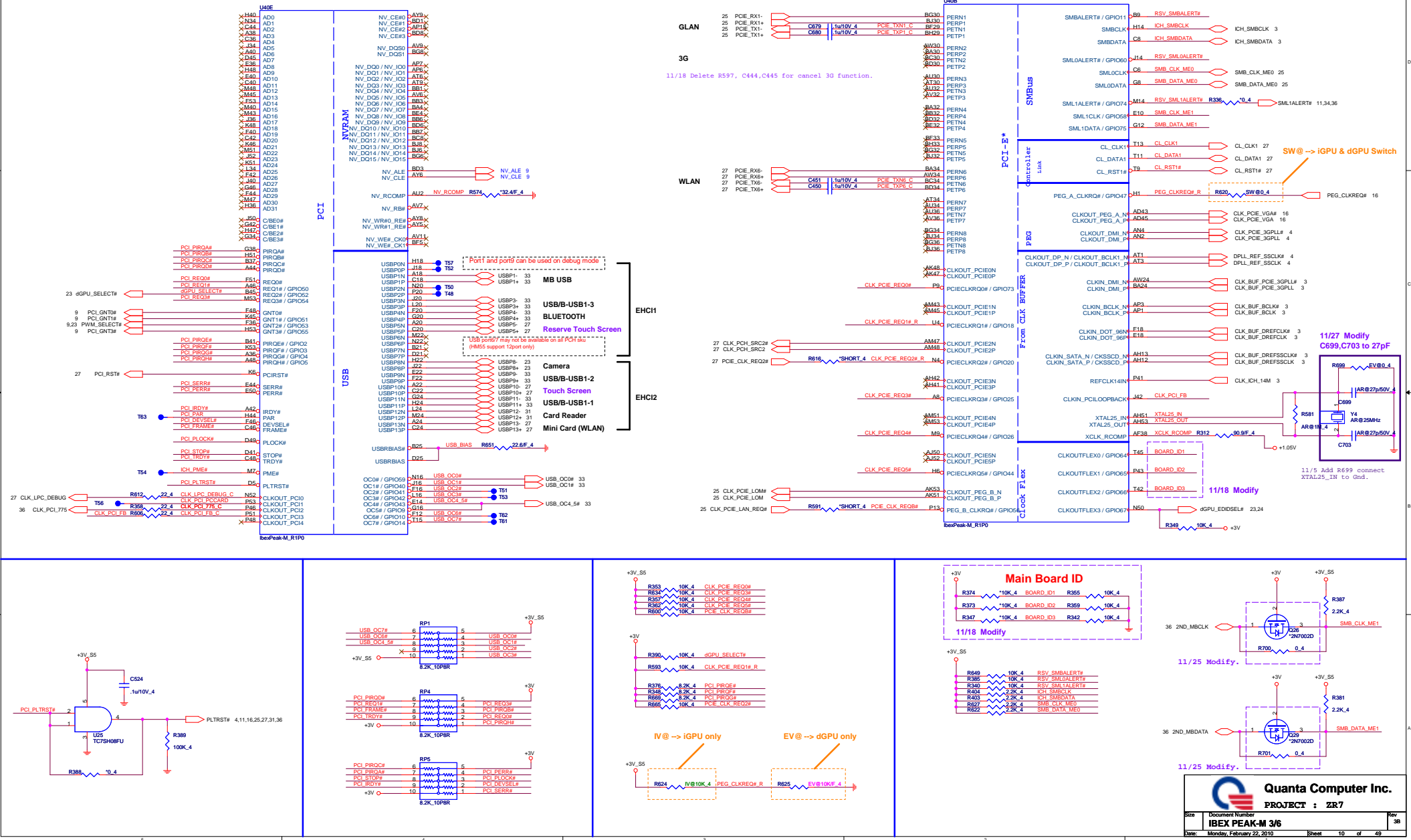
HDA\_SYNC (PCH strap pin)  
Internal weak pull-down  
VCCVRM=>+1.8V (default)  
external pull-up  
VCCVRM=>+1.5V



PCH Strap Pin Configuration Table-1

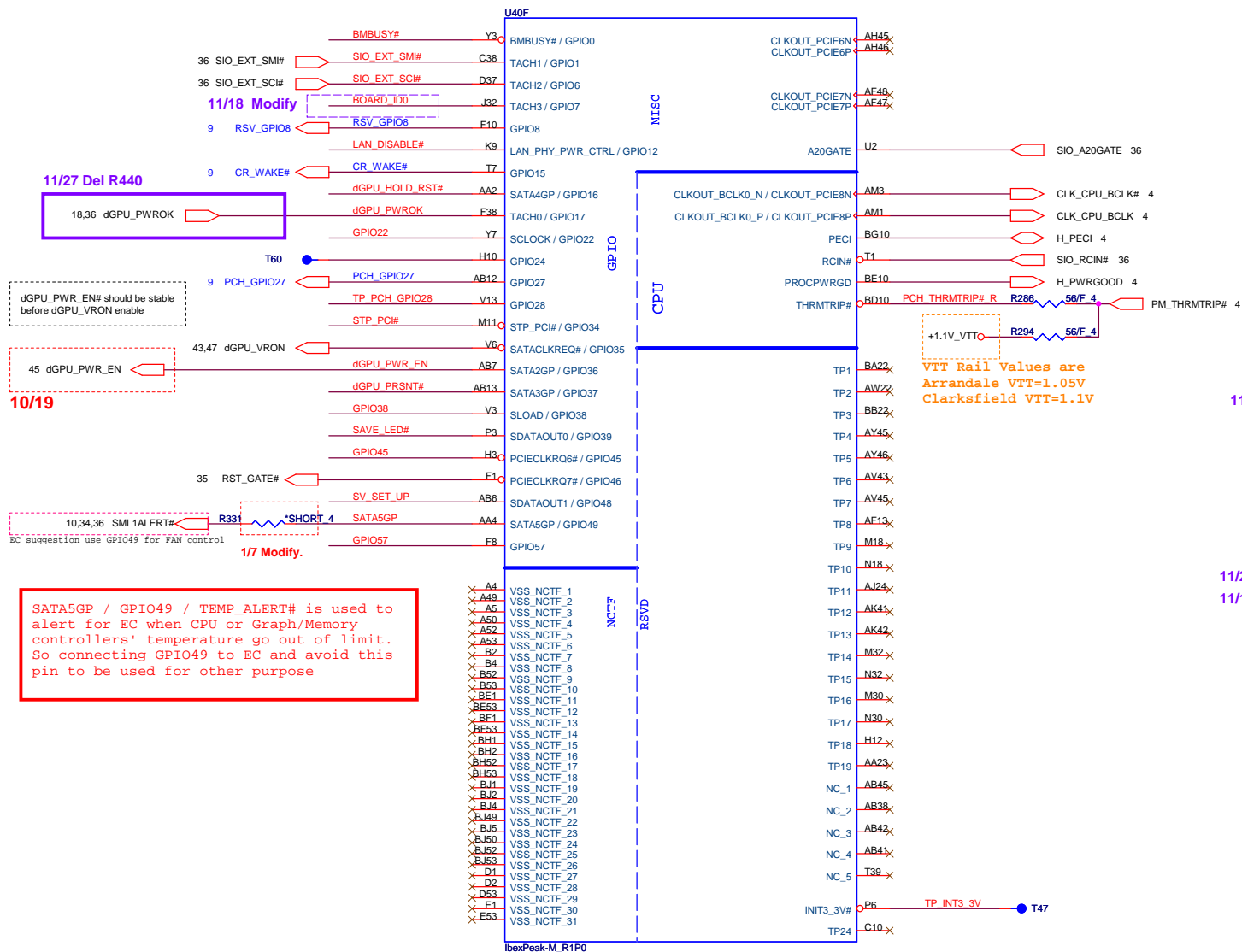
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC - R685 330K 6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disabled	+3V - R618 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V - R611 1K 4 4SPKR
HDA_DOCK# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled	PCH_GPIO33 - R370 1K 4 +3V R382 10K 4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	PCH_GNT0# - R360 1K 4 PCH_GNT1# - R363 1K 4 PCH_GNT1# - R708 1K 4 PCH_GNT1# - R709 1K 4
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	10,23 PWM_SELECT# - R364 1K 4
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCH_GNT3# - R628 10K 4
NV_ALE	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE - R296 1K 4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE - R295 1K 4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPIO8 - R380 10K 4 +3V_S5 R371 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# - R341 1K 4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 - R324 10K 4

IV@ --> iGPU only  
EV@ --> dGPU only  
SW@ --> iGPU & dGPU Switch

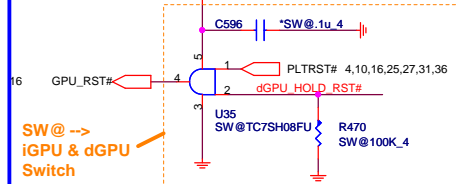


IV@ --> iGPU only  
 EV@ --> dGPU only  
 SW@ --> iGPU & dGPU Switch  
 ES@ --> External VGA SKU

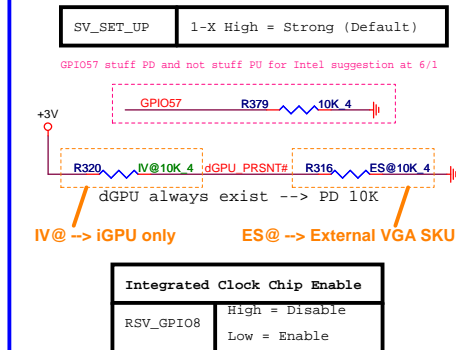
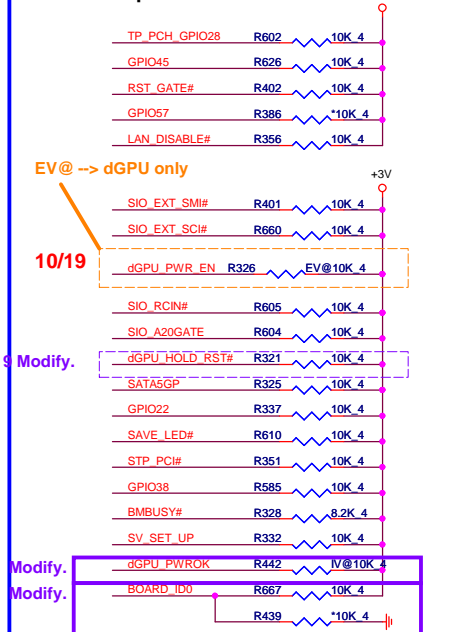
## IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



### GPU RST#

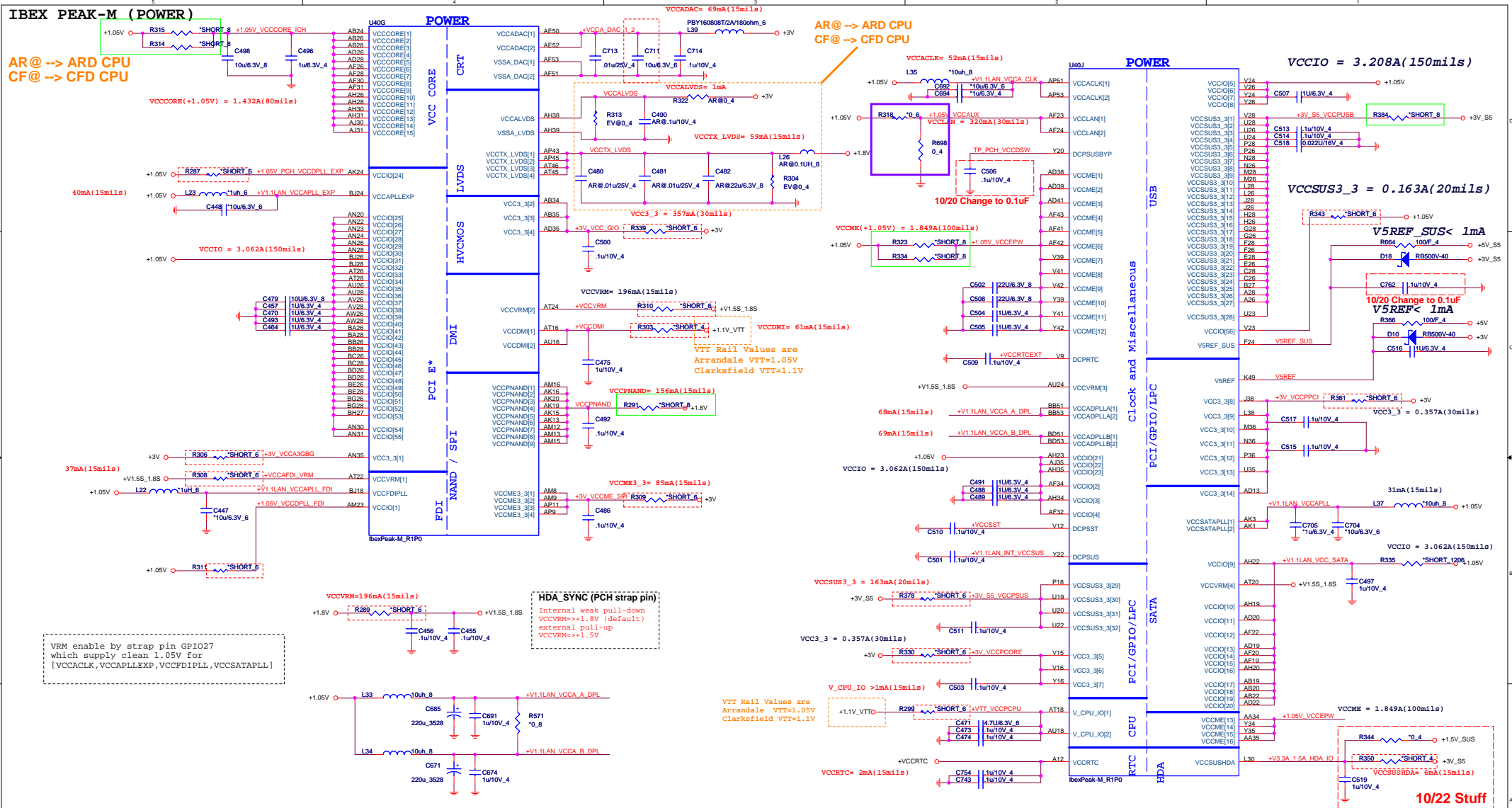


### GPIO Pull-up/Pull-down





AR@ --> ARD CPU  
CF@ --> CFD CPU



**Quanta Computer Inc.**  
**PROJECT : ZR7**

Size	Document Number <b>IBEX PEAK-M 5/6</b>	Rev	3B
Date	Monday, February 22, 2010	Sheet	12 of 49

# IBEX PEAK-M (GND)


U40H		
AB16	VSS[0]	
AA19	VSS[1]	VSS[80] AK30
AA20	VSS[2]	VSS[81] AK31
AA22	VSS[3]	VSS[82] AK32
AM19	VSS[4]	VSS[83] AK33
AA24	VSS[5]	VSS[84] AK34
AA26	VSS[6]	VSS[85] AK35
AA28	VSS[7]	VSS[86] AK36
AA30	VSS[8]	VSS[87] AK37
AA31	VSS[9]	VSS[88] AK38
AA32	VSS[10]	VSS[89] AK39
AB11	VSS[11]	VSS[90] AK40
AB15	VSS[12]	VSS[91] AK41
AB23	VSS[13]	VSS[92] AK42
AB30	VSS[14]	VSS[93] AK43
AB31	VSS[15]	VSS[94] AK44
AB32	VSS[16]	VSS[95] AK45
AB39	VSS[17]	VSS[96] AK46
AB43	VSS[18]	VSS[97] AK47
AB47	VSS[19]	VSS[98] AK48
AB5	VSS[20]	VSS[99] AK49
AB8	VSS[21]	VSS[100] AK50
AC2	VSS[22]	VSS[101] AK51
AC22	VSS[23]	VSS[102] AK52
AD11	VSS[24]	VSS[103] AK53
AD12	VSS[25]	VSS[104] AK54
AD16	VSS[26]	VSS[105] AK55
AD23	VSS[27]	VSS[106] AK56
AD30	VSS[28]	VSS[107] AK57
AD31	VSS[29]	VSS[108] AK58
AD32	VSS[30]	VSS[109] AK59
AD34	VSS[31]	VSS[110] AK60
AJ22	VSS[32]	VSS[111] AK61
AD42	VSS[33]	VSS[112] AK62
AD46	VSS[34]	VSS[113] AK63
AD49	VSS[35]	VSS[114] AK64
AD7	VSS[36]	VSS[115] AK65
AE2	VSS[37]	VSS[116] AK66
AE4	VSS[38]	VSS[117] AK67
AE12	VSS[39]	VSS[118] AK68
Y13	VSS[40]	VSS[119] AK69
AH49	VSS[41]	VSS[120] AK70
AU4	VSS[42]	VSS[121] AK71
AF35	VSS[43]	VSS[122] AK72
AP13	VSS[44]	VSS[123] AK73
AN34	VSS[45]	VSS[124] AK74
AE45	VSS[46]	VSS[125] AK75
AF46	VSS[47]	VSS[126] AK76
AF49	VSS[48]	VSS[127] AK77
AF5	VSS[49]	VSS[128] AK78
AF8	VSS[50]	VSS[129] AK79
AG2	VSS[51]	VSS[130] AK80
AG52	VSS[52]	VSS[131] AK81
AH11	VSS[53]	VSS[132] AK82
AH15	VSS[54]	VSS[133] AK83
AH16	VSS[55]	VSS[134] AK84
AH24	VSS[56]	VSS[135] AK85
AH32	VSS[57]	VSS[136] AK86
AV18	VSS[58]	VSS[137] AK87
AH43	VSS[59]	VSS[138] AK88
AH47	VSS[60]	VSS[139] AK89
AH7	VSS[61]	VSS[140] AK90
AJ2	VSS[62]	VSS[141] AK91
AJ19	VSS[63]	VSS[142] AK92
AJ20	VSS[64]	VSS[143] AK93
AJ22	VSS[65]	VSS[144] AK94
AJ23	VSS[66]	VSS[145] AK95
AJ26	VSS[67]	VSS[146] AK96
AJ28	VSS[68]	VSS[147] AK97
AJ32	VSS[69]	VSS[148] AK98
AJ34	VSS[70]	VSS[149] AK99
AT5	VSS[71]	VSS[150] AK100
AJ4	VSS[72]	VSS[151] AK101
AK12	VSS[73]	VSS[152] AK102
AM41	VSS[74]	VSS[153] AK103
AN19	VSS[75]	VSS[154] AK104
AK26	VSS[76]	VSS[155] AK105
AK22	VSS[77]	VSS[156] AK106
AK23	VSS[78]	VSS[157] AK107
AK28	VSS[79]	VSS[158] AK108

IbexPeak-M\_R1P0

## U40I

AY7	VSS[159]	VSS[259] H49
B11	VSS[160]	VSS[260] H5
B15	VSS[161]	VSS[261] J24
B19	VSS[162]	VSS[262] K11
B23	VSS[163]	VSS[263] K43
B31	VSS[164]	VSS[264] K47
B35	VSS[165]	VSS[265] L14
B39	VSS[166]	VSS[266] L18
B43	VSS[167]	VSS[267] L2
B47	VSS[168]	VSS[268] L22
B7	VSS[169]	VSS[269] L32
BG12	VSS[170]	VSS[270] L36
BB12	VSS[171]	VSS[271] L40
BB16	VSS[172]	VSS[272] L52
BB20	VSS[173]	VSS[273] M12
BB24	VSS[174]	VSS[274] M16
BB30	VSS[175]	VSS[275] M20
BB34	VSS[176]	VSS[276] M34
BB38	VSS[177]	VSS[277] M38
BB42	VSS[178]	VSS[278] M42
BB49	VSS[179]	VSS[279] M46
BB5	VSS[180]	VSS[280] M49
BC10	VSS[181]	VSS[281] M5
BC14	VSS[182]	VSS[282] M8
BC18	VSS[183]	VSS[283] N24
BC2	VSS[184]	VSS[284] P11
BC22	VSS[185]	VSS[285] AD15
BC32	VSS[186]	VSS[286] P22
BC36	VSS[187]	VSS[287] P30
BC40	VSS[188]	VSS[288] P32
BC44	VSS[189]	VSS[289] P34
BC52	VSS[190]	VSS[290] P42
BH9	VSS[191]	VSS[291] P45
BD48	VSS[192]	VSS[292] P47
BD49	VSS[193]	VSS[293] R2
BD5	VSS[194]	VSS[294] R52
BE12	VSS[195]	VSS[295] T12
BE16	VSS[196]	VSS[296] T41
BE20	VSS[197]	VSS[297] T46
BE24	VSS[198]	VSS[298] T49
BE30	VSS[199]	VSS[299] T5
BE34	VSS[200]	VSS[300] T8
BE38	VSS[201]	VSS[301] U30
BE42	VSS[202]	VSS[302] U32
BE46	VSS[203]	VSS[303] U34
BE48	VSS[204]	VSS[304] U36
BE50	VSS[205]	VSS[305] U38
BE6	VSS[206]	VSS[306] V11
BE8	VSS[207]	VSS[307] P16
BF3	VSS[208]	VSS[308] V19
BF49	VSS[209]	VSS[309] V20
BF51	VSS[210]	VSS[310] V22
BG18	VSS[211]	VSS[311] V30
BG24	VSS[212]	VSS[312] V31
BG4	VSS[213]	VSS[313] V32
BC50	VSS[214]	VSS[314] V34
BH11	VSS[215]	VSS[315] V43
BH15	VSS[216]	VSS[316] V45
BH19	VSS[217]	VSS[317] V46
BH23	VSS[218]	VSS[318] V47
BH31	VSS[219]	VSS[319] V49
BH35	VSS[220]	VSS[320] V5
BH39	VSS[221]	VSS[321] V7
BH43	VSS[222]	VSS[322] V8
BH47	VSS[223]	VSS[323] W2
BH7	VSS[224]	VSS[324] W52
C12	VSS[225]	VSS[325] Y11
C50	VSS[226]	VSS[326] Y12
D51	VSS[227]	VSS[327] Y15
E12	VSS[228]	VSS[328] Y19
E16	VSS[229]	VSS[329] Y23
E20	VSS[230]	VSS[330] Y28
E24	VSS[231]	VSS[331] Y30
E30	VSS[232]	VSS[332] Y31
E34	VSS[233]	VSS[333] Y32
E38	VSS[234]	VSS[334] Y38
E42	VSS[235]	VSS[335] Y43
E46	VSS[236]	VSS[336] Y46
E48	VSS[237]	VSS[337] P49
E6	VSS[238]	VSS[338] Y5
F8	VSS[239]	VSS[339] Y6
F49	VSS[240]	VSS[340] Y8
F5	VSS[241]	VSS[341] P24
G10	VSS[242]	VSS[342] T43
G14	VSS[243]	VSS[343] AD51
G18	VSS[244]	VSS[344] ATR
G2	VSS[245]	VSS[345] AD47
G22	VSS[246]	VSS[346] Y47
G32	VSS[247]	VSS[347] AT12
G36	VSS[248]	VSS[348] AM6
G40	VSS[249]	VSS[349] AT13
G44	VSS[250]	VSS[350] AM5
G52	VSS[251]	VSS[351] AK45
AF39	VSS[252]	VSS[352] AK38
H16	VSS[253]	VSS[353] AV14
H20	VSS[254]	
H30	VSS[255]	
H34	VSS[256]	
H38	VSS[257]	
H42	VSS[258]	

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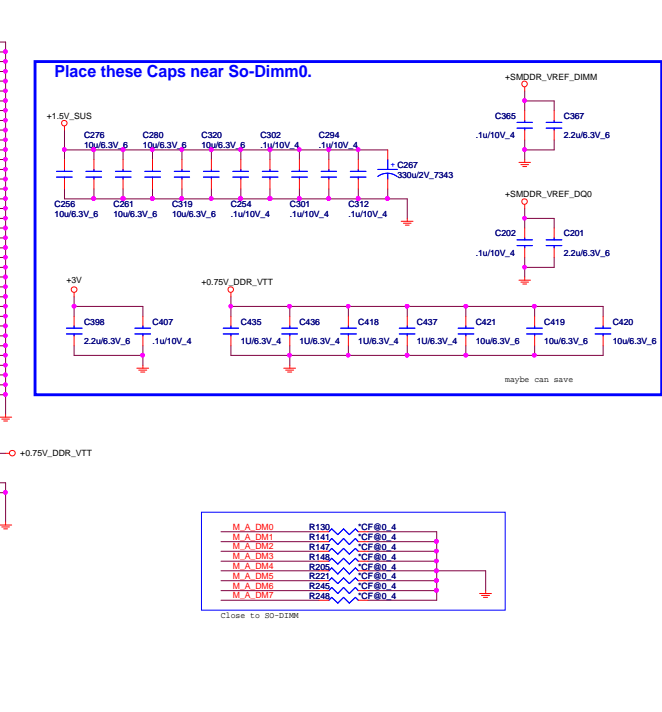
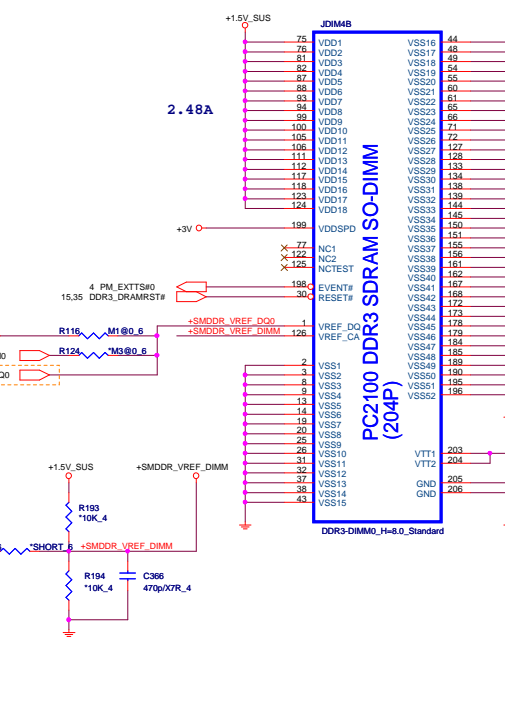
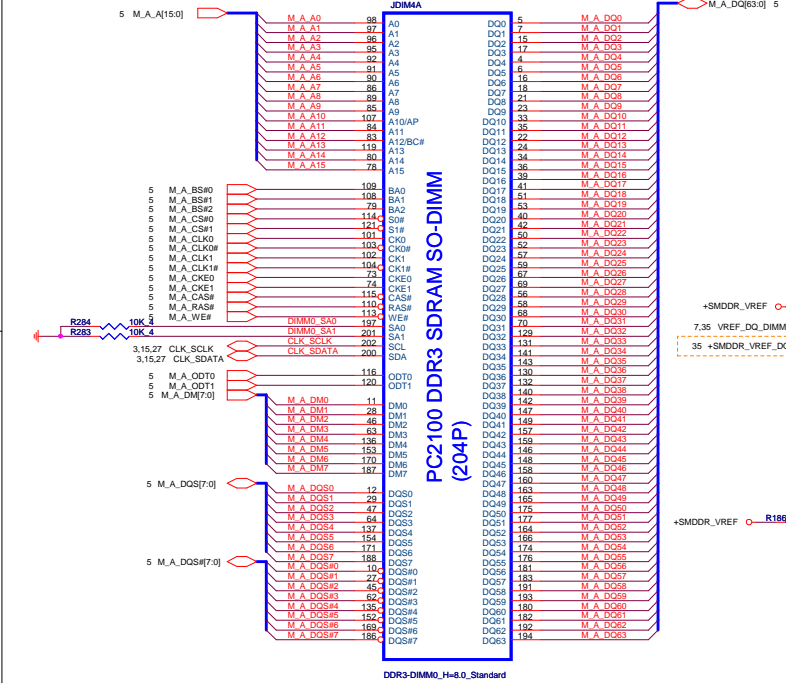
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PROJECT : ZR7

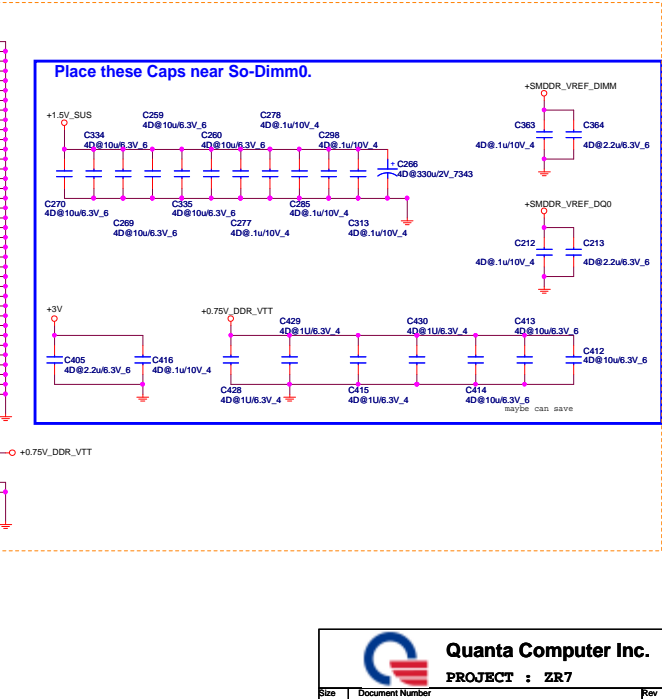
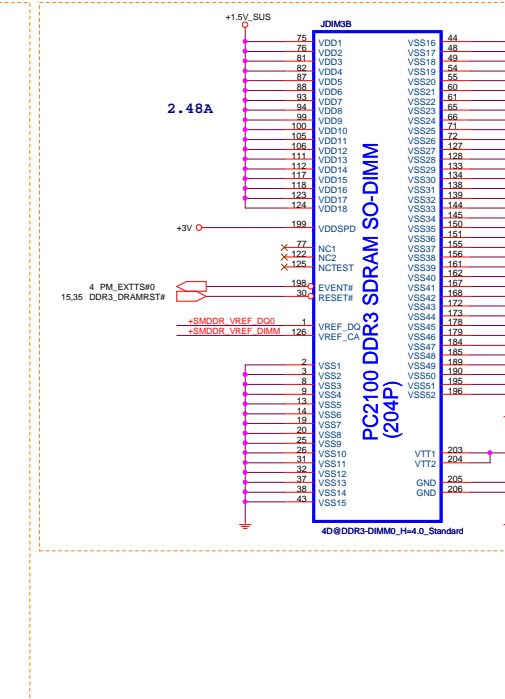
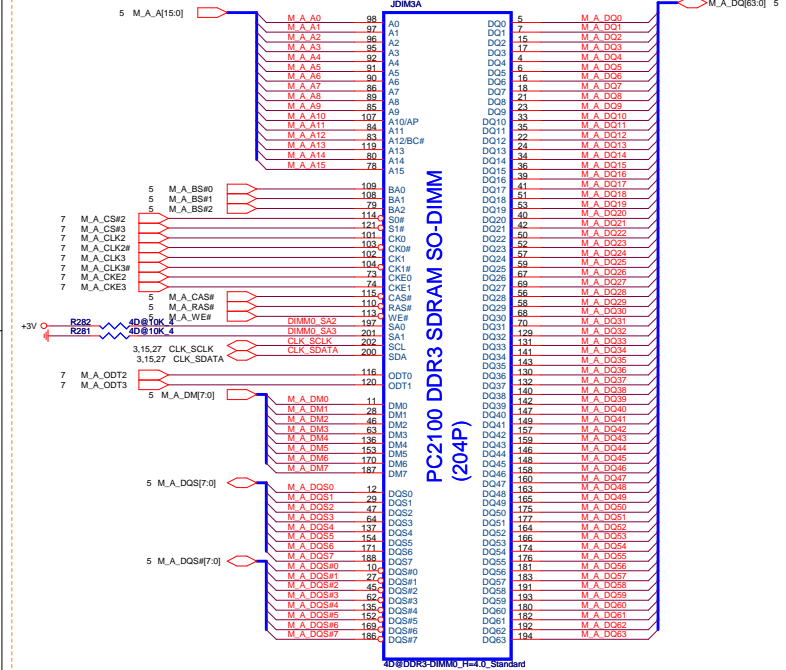
Size	Document Number	Rev
	<b>IBEX PEAK-M 6/6</b>	<b>3B</b>
Date:	Monday, February 22, 2010	Sheet 13 of 49



## DIMM A0

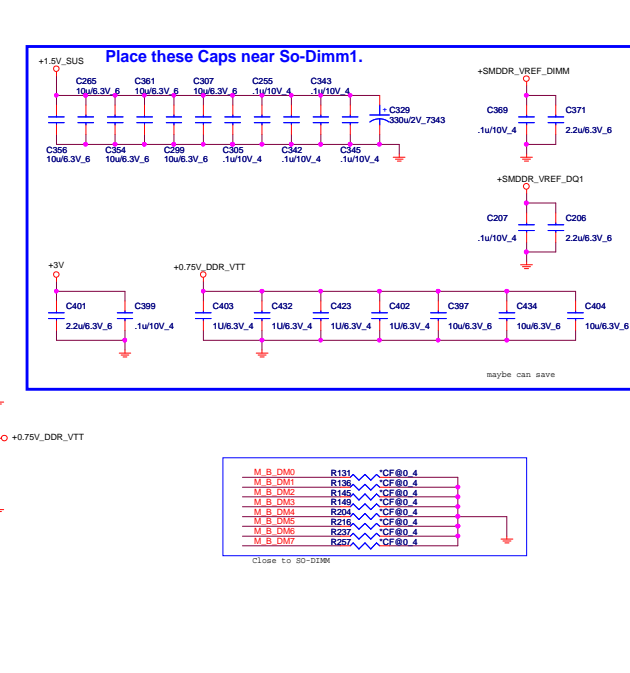
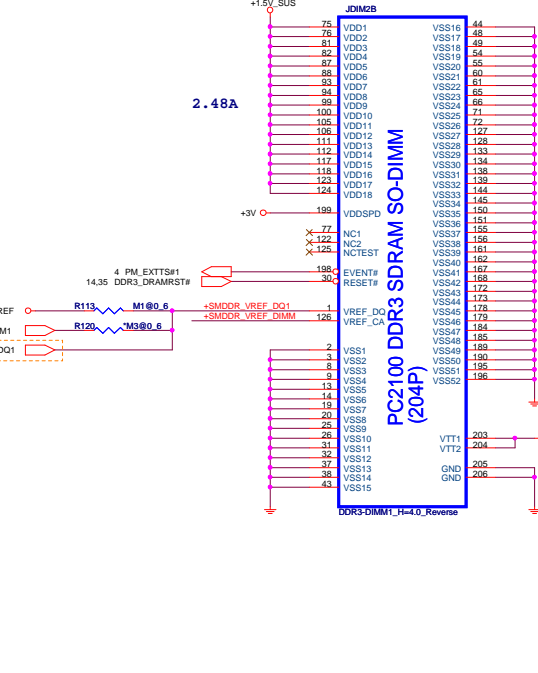
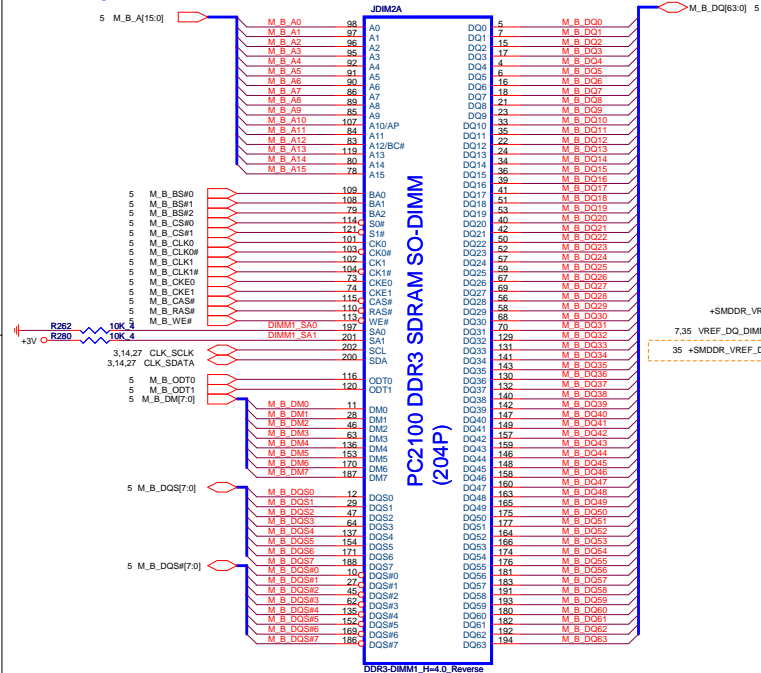


## DIMM A1 4D@ -> 4 SO-DIMM

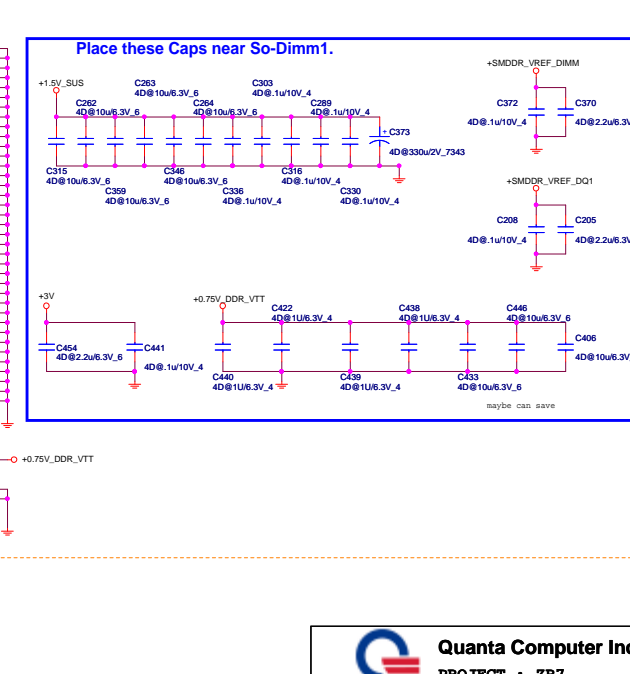
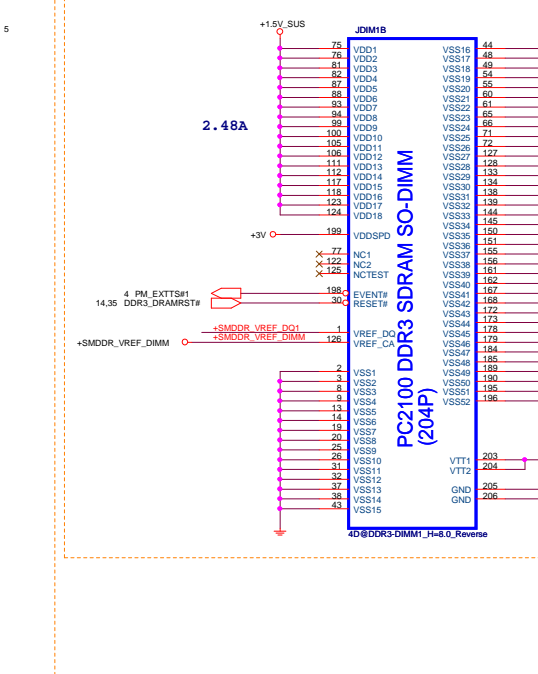
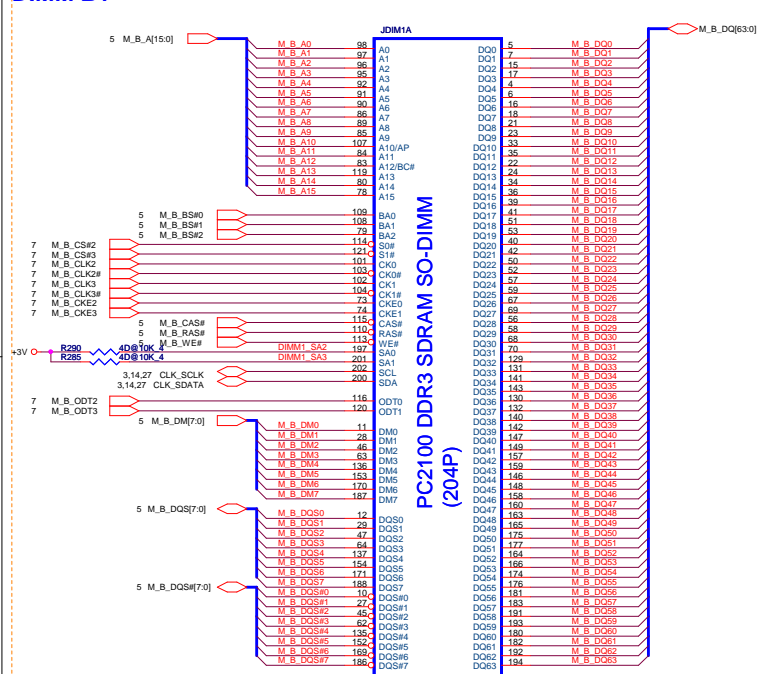




## DIMM B0



## DIMM B1 4D@ --> 4 SO-DIMM



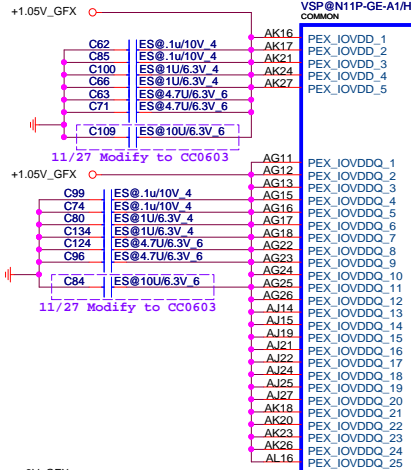
PEX\_IOVDD+PEX\_IOVDDQ+PEX\_PLLVDD >2.2A

~ 500mA

1600mA

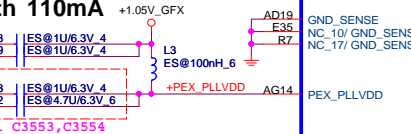
Near BGA

U33A  
VSP@N11P-GE-A1/H  
COMMON

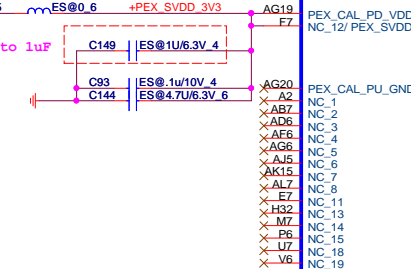


PCI EXPRESS

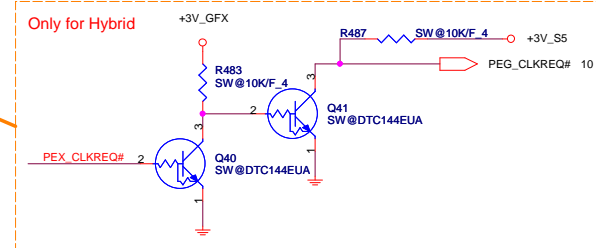
12~16 mils width 110mA



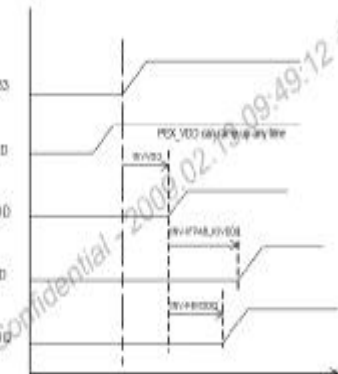
12~16 mils width



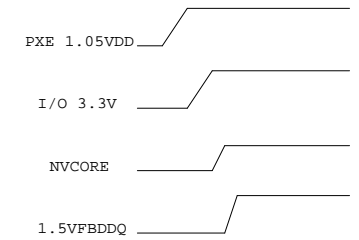
SW @ --> iGPU & dGPU Switch



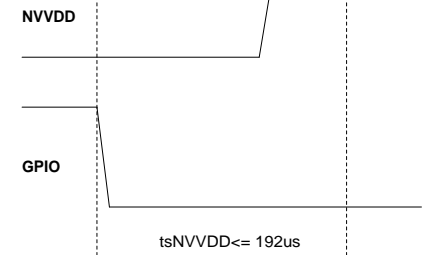
EV @ --> dGPU only  
SW @ --> iGPU & dGPU Switch  
ES @ --> External VGA SKU  
VSP @ --> Operation P/N (VGA)



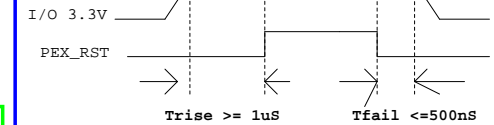
power up sequence



NB9M: VGACORE +0.90V (Normal), +1.09V  
NVVDD Maximum Settling Time



PEX\_RST timing



**Quanta Computer Inc.**  
PROJECT : ZR7

Size	Document Number	Rev
	N11P-GE (PCIE I/F) 1/5	3B
Date:	Monday, February 22, 2010	Sheet 16 of 49

VSP@ --> Operation P/N (VGA) 11EP@ --> N11P/N11E-GE1 Setting  
ES@ --> External VGA SKU U33B 12/1

U33B

12/02 modify  
package for N10

21 VMA\_DQ[63..0]

21 VMA\_DM[7..0]

21 VMA\_WDQS[7..0]

21 VMA\_RDQS[7..0]

22 VMC\_DQ[63..0]

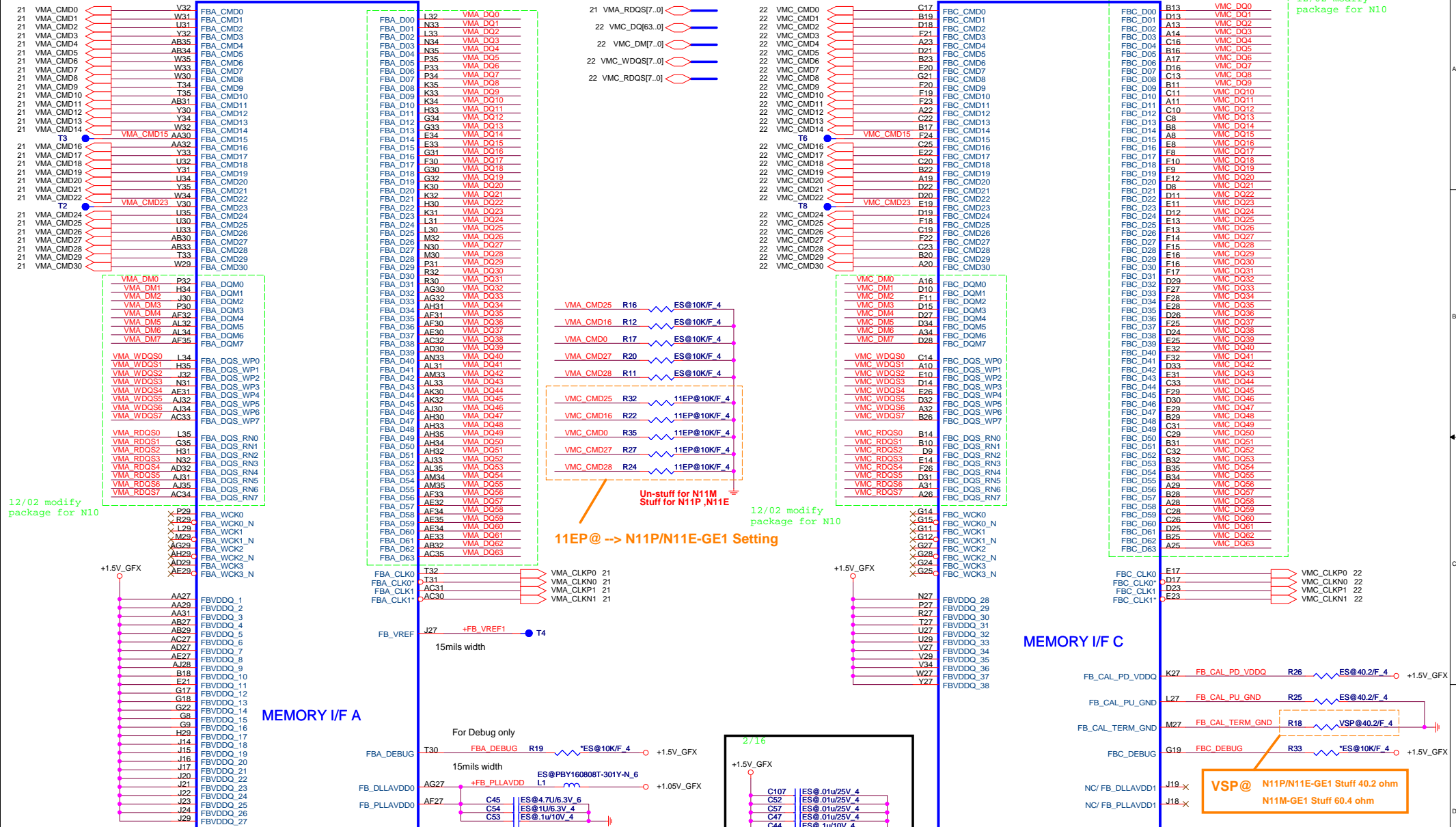
22 VMC\_DM[7..0]


22 VMC\_WDQS[7..0]

22 VMC\_RDQS[7..0]

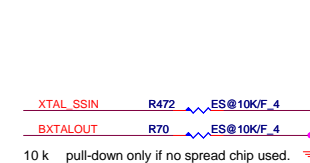
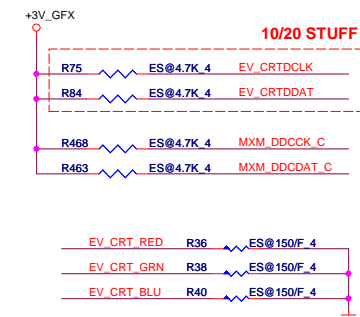
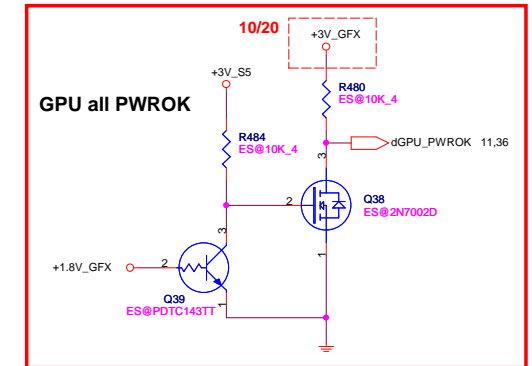
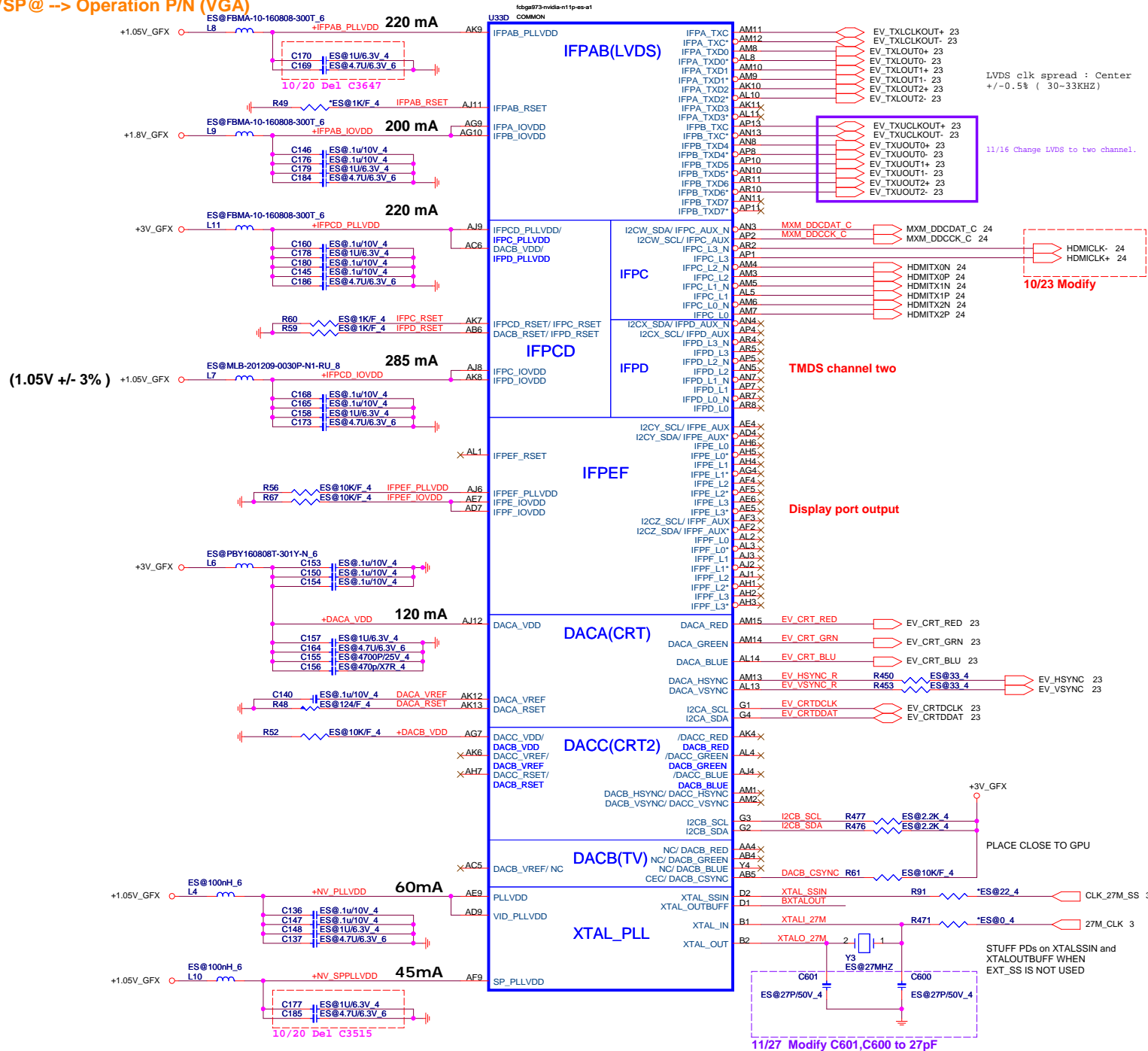
U33C

12/02 modify  
package for N10



 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		
Size	Document Number	Rev
	<b>N11P-GE (MEMORY I/F) 2/5</b>	<b>3B</b>
Date:	Monday, February 22, 2010	Sheet 17 of 49

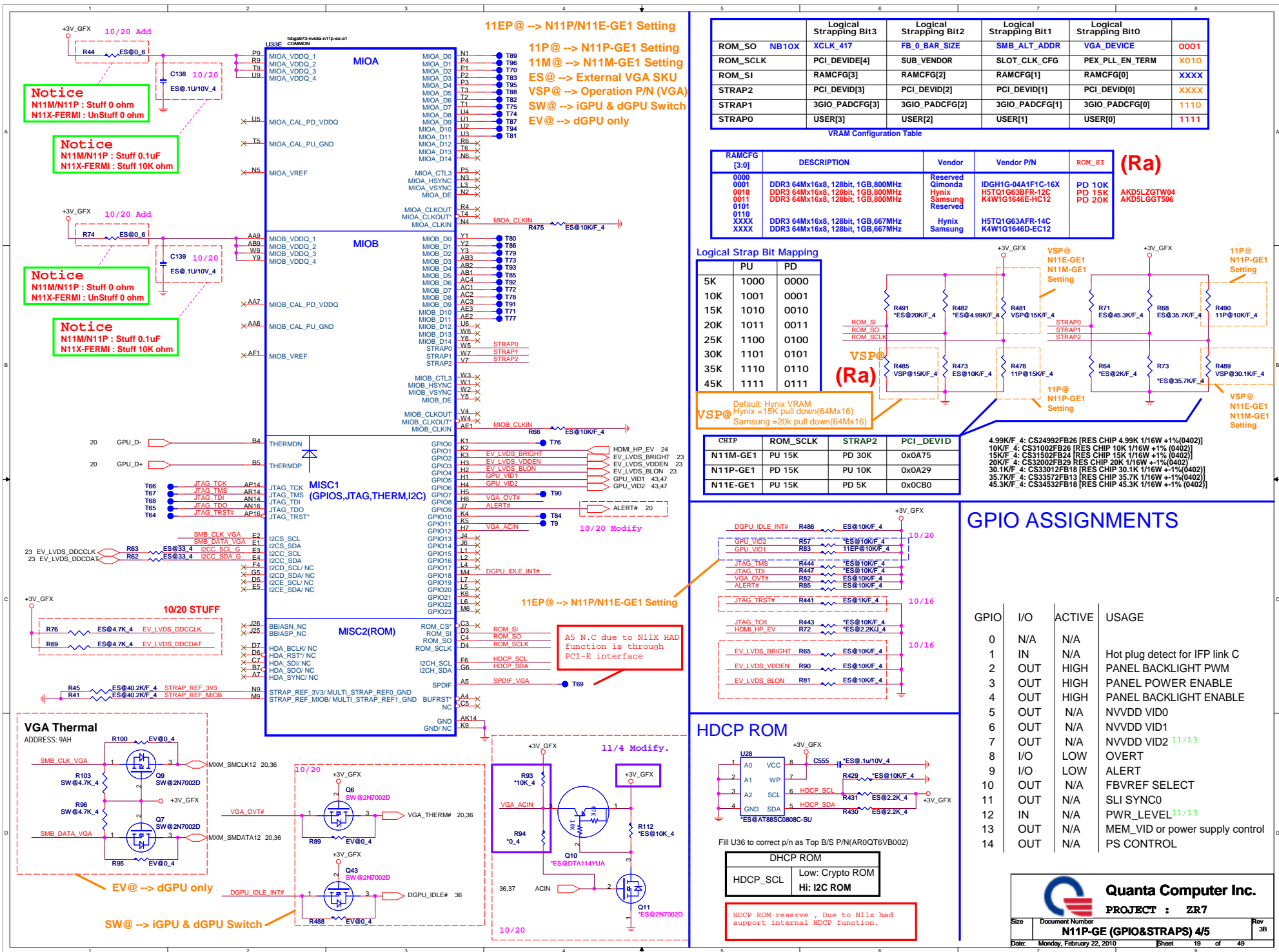
ES@ --> External VGA SKU  
VSP@ --> Operation P/N (VGA)



**Quanta Computer Inc.**  
**PROJECT : ZR7**

Size	Document Number <b>N11P-GE (DISPLAY) 3/5</b>	Rev 3B
Date:	Monday, February 22, 2010	Sheet 18 of 49

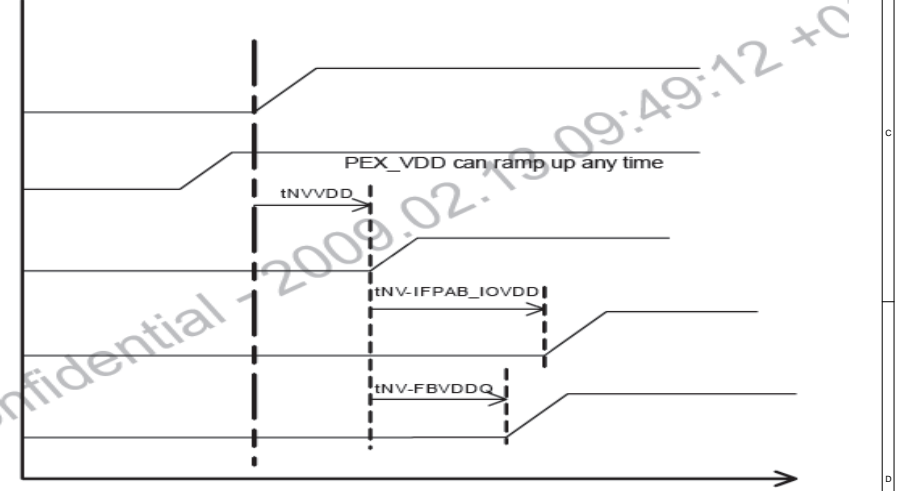
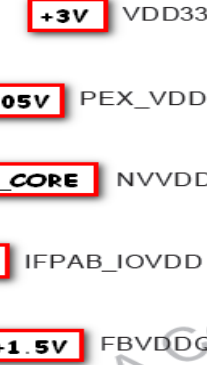
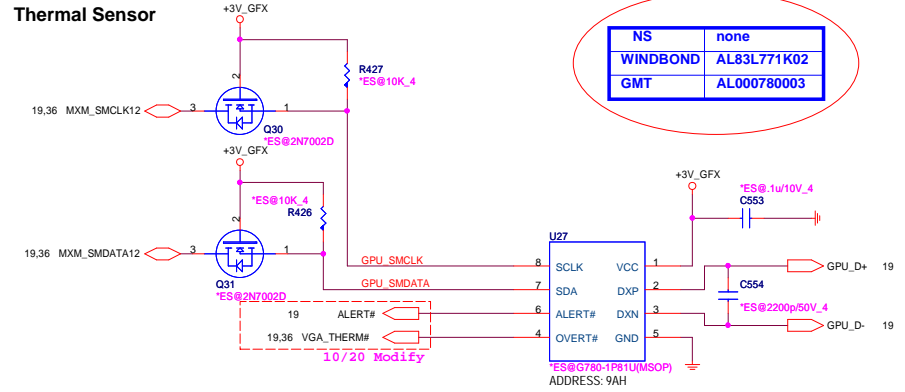




ES@ --> External VGA SKU  
VSP@ --> Operation P/N (VGA)

# Thermal Sensor

NS	none
WINDBOND	AL83L771K02
GMT	AL000780003



Quanta Computer Inc.  
PROJECT : ZR7  
N11P-GE (POWER & GND&THM) 5/5  
Date: Monday, February 22, 2010 Sheet 20 of 49

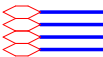


**VSP@ --> Operation P/N (VGA-VRAM)**

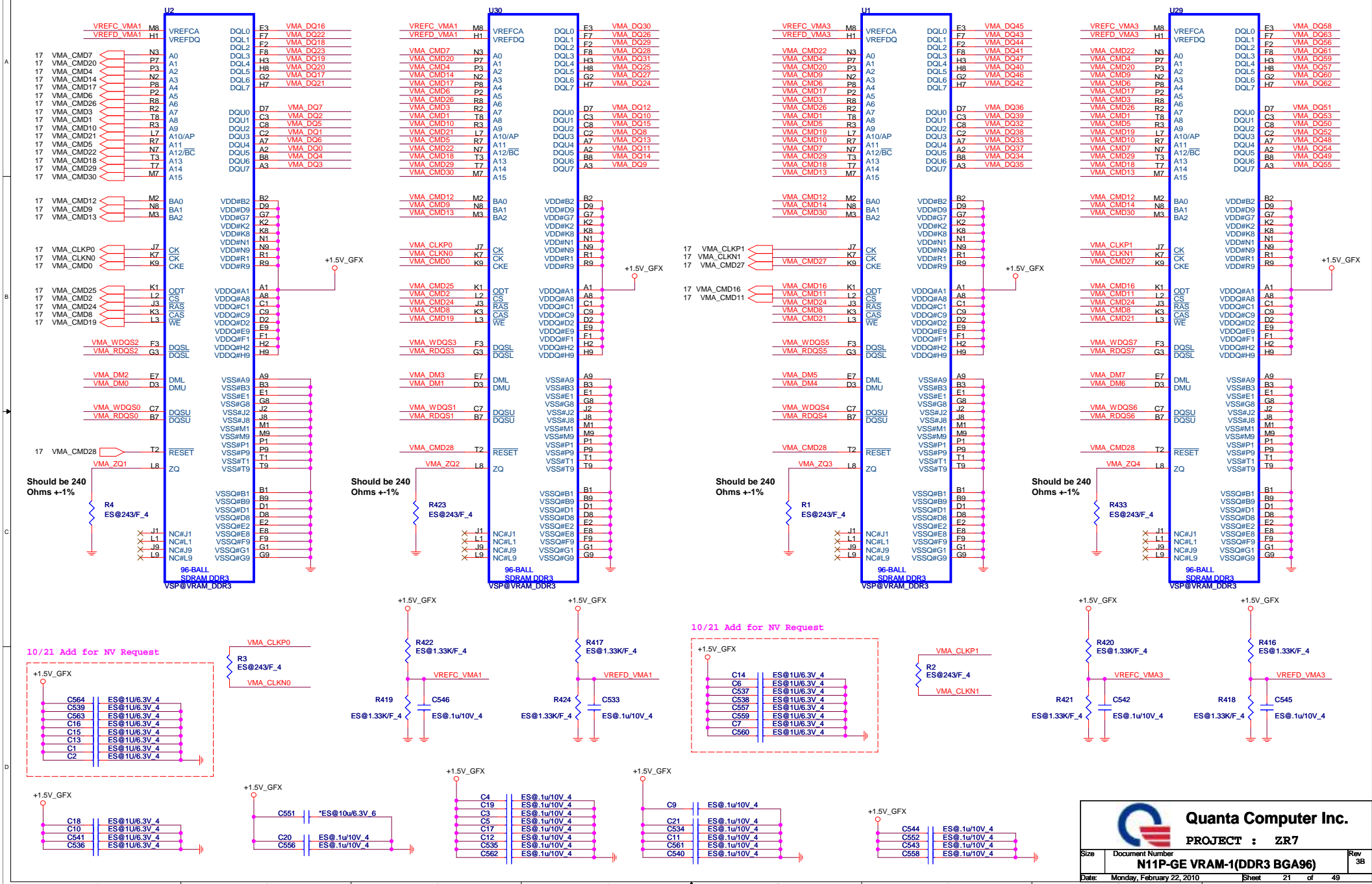
```

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

```

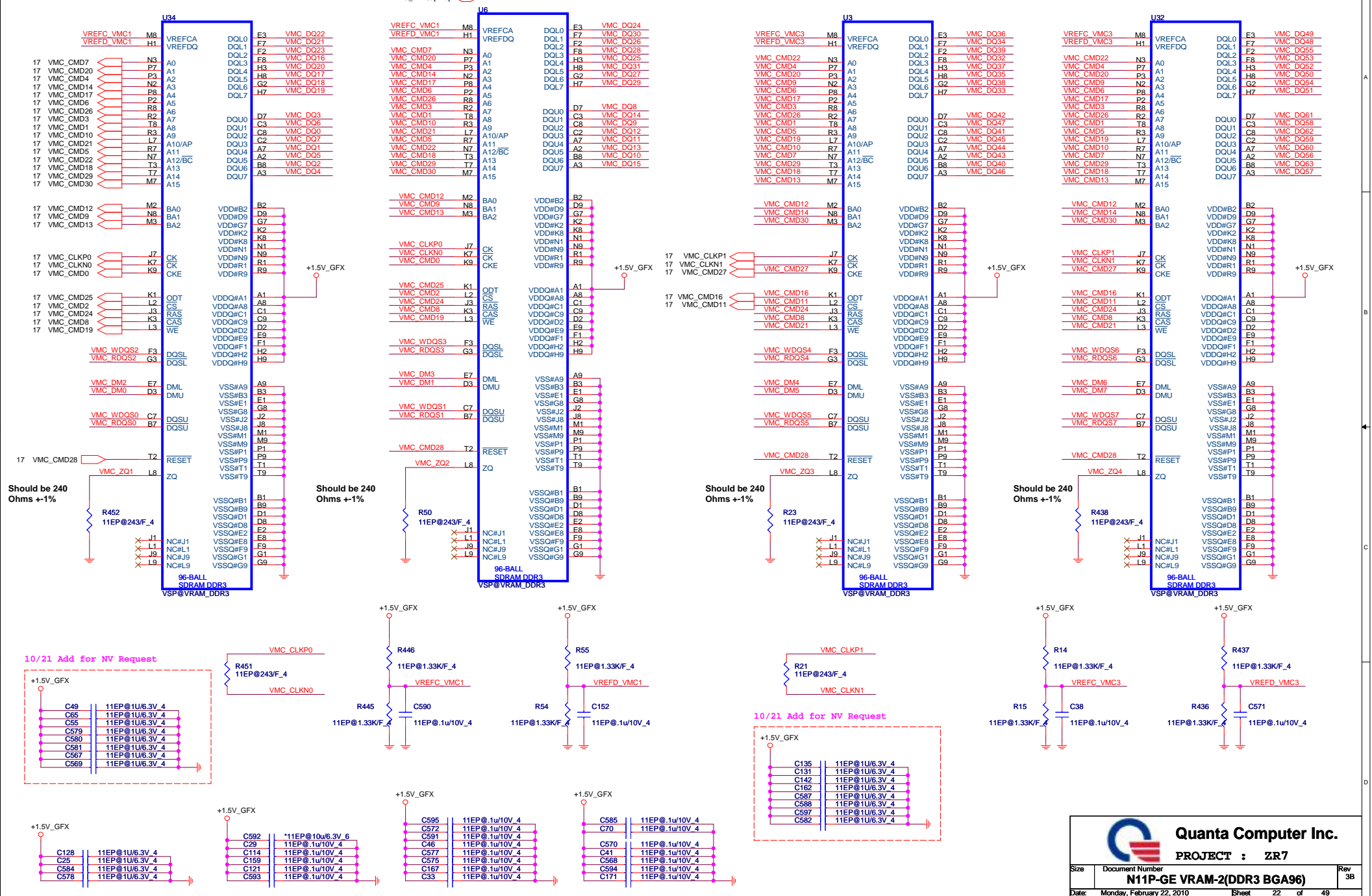


**CHANNEL A: 256MB/512MB DDR3**



**VSP@ --> Operation P/N (VGA-VRAM CH:B N11P/N11E only)**

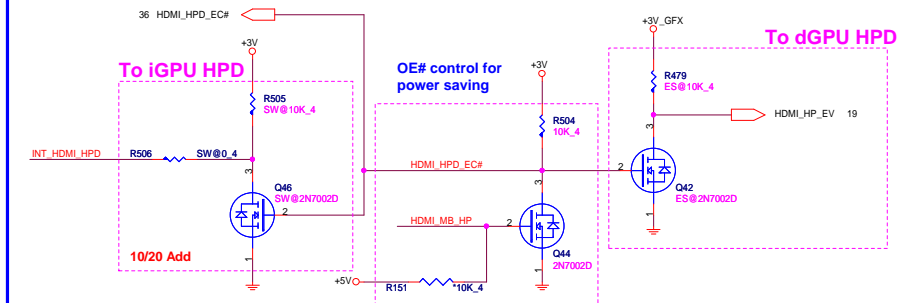
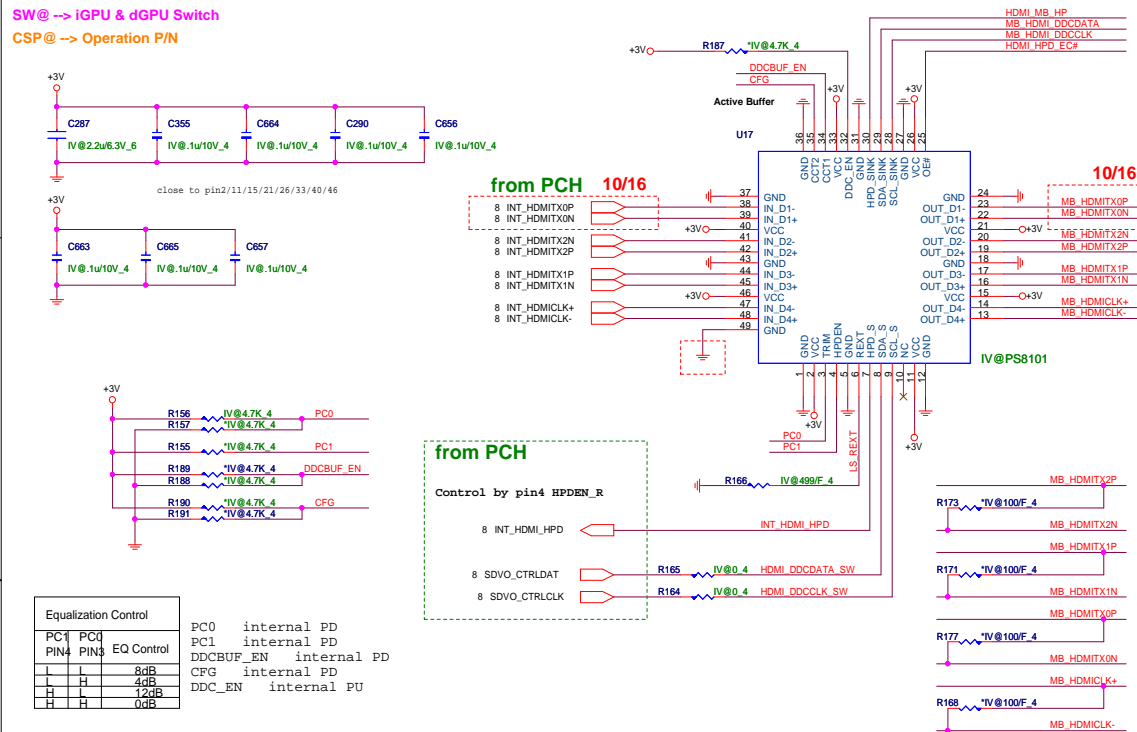
**CHANNEL B: 256MB/512MB DDR3**



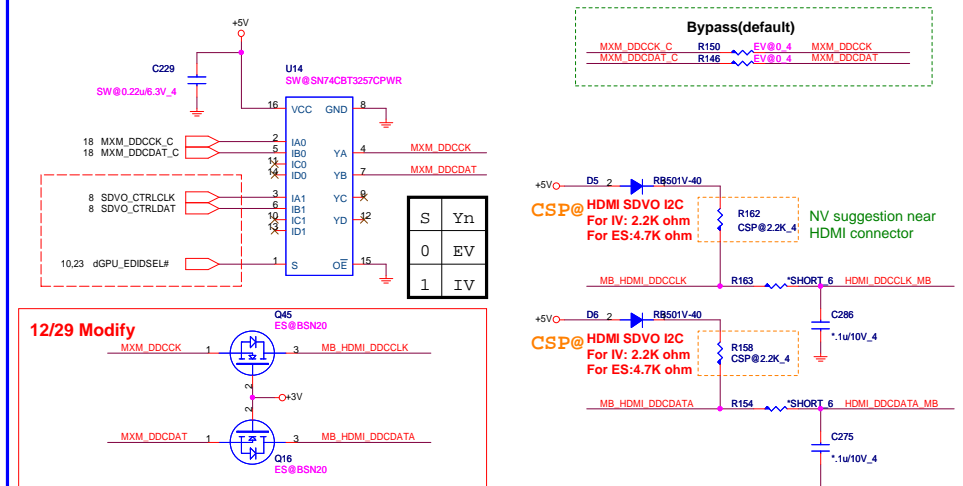


## iGPU HDMI LEVEL SHIFTER

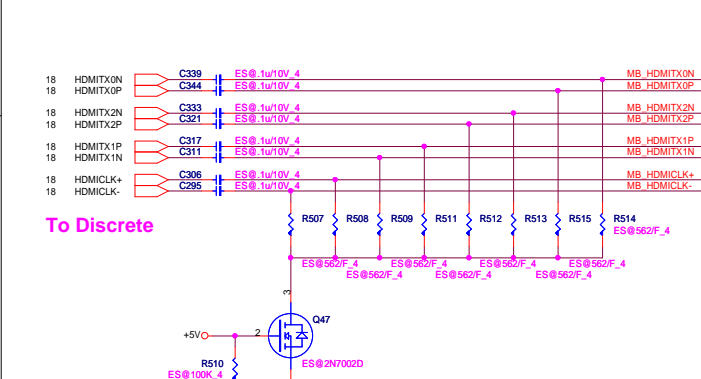
IV@ -> iGPU only  
 EV@ -> dGPU only  
 ES@ -> External VGA SKU  
 SW@ -> iGPU & dGPU Switch  
 CSP@ -> Operation P/N



## SDVO I2C Control



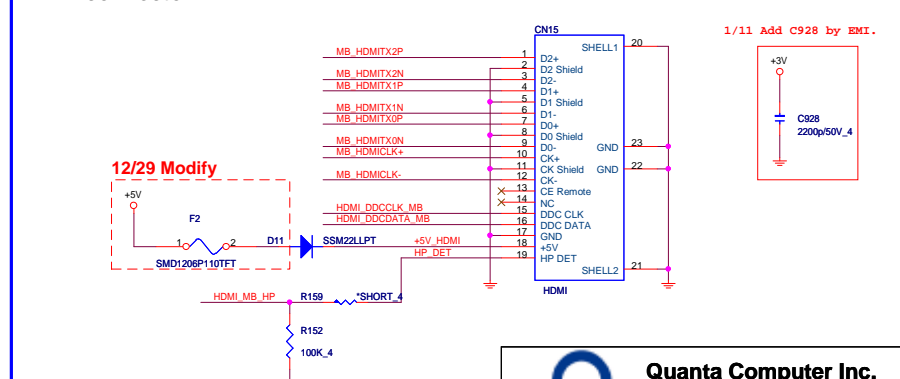
## GPU Switchable Graphic HDMI source



## ESD Protect

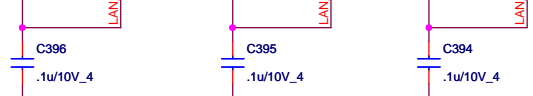
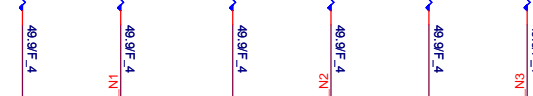
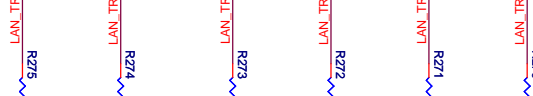
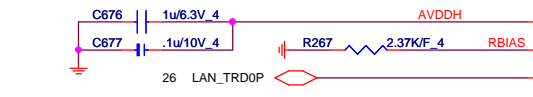
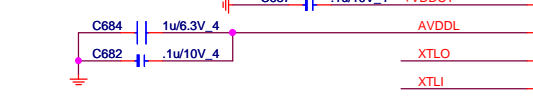
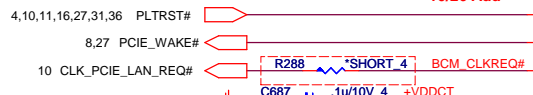
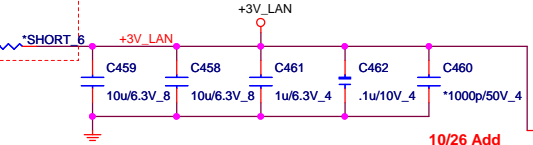
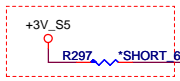
12/29 Delete U15, U16, U18.

## HDMI connector

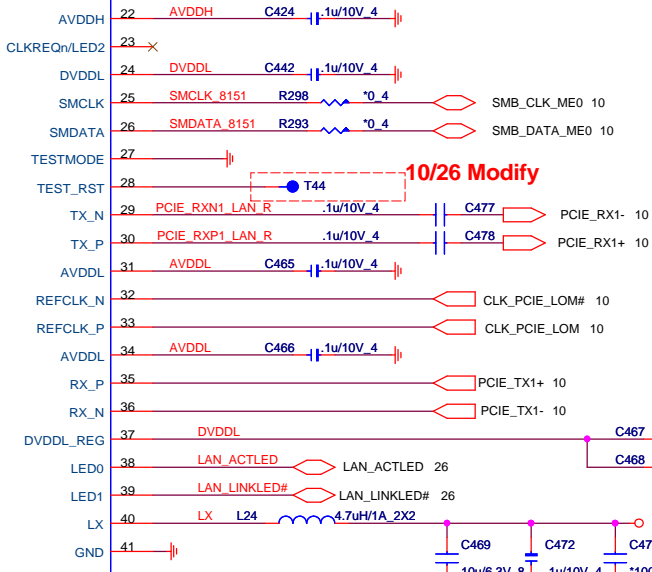


# Giga-LAN AR8151

10/26 Add



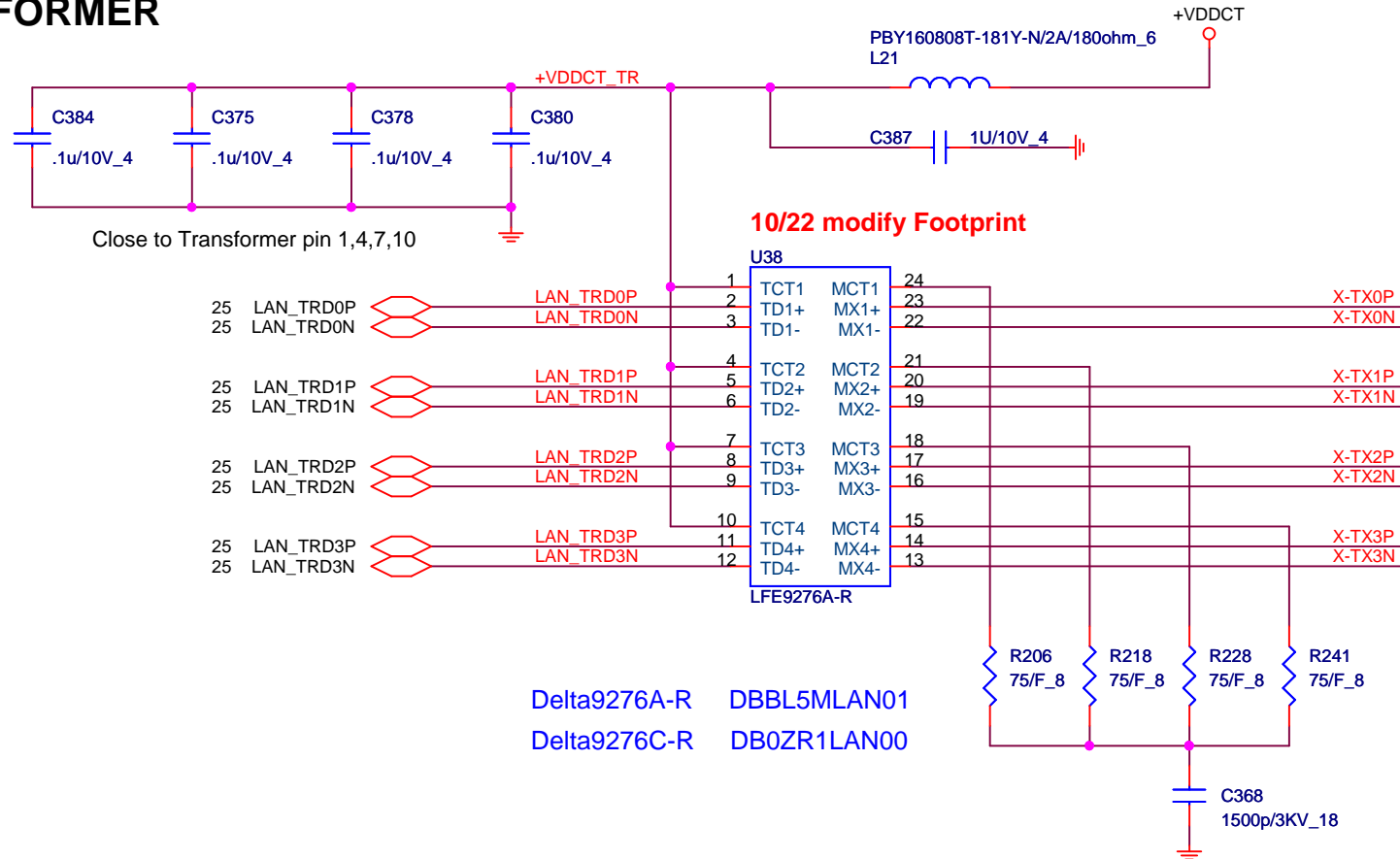
AR8151  
5X5mm  
40-Pin QFN



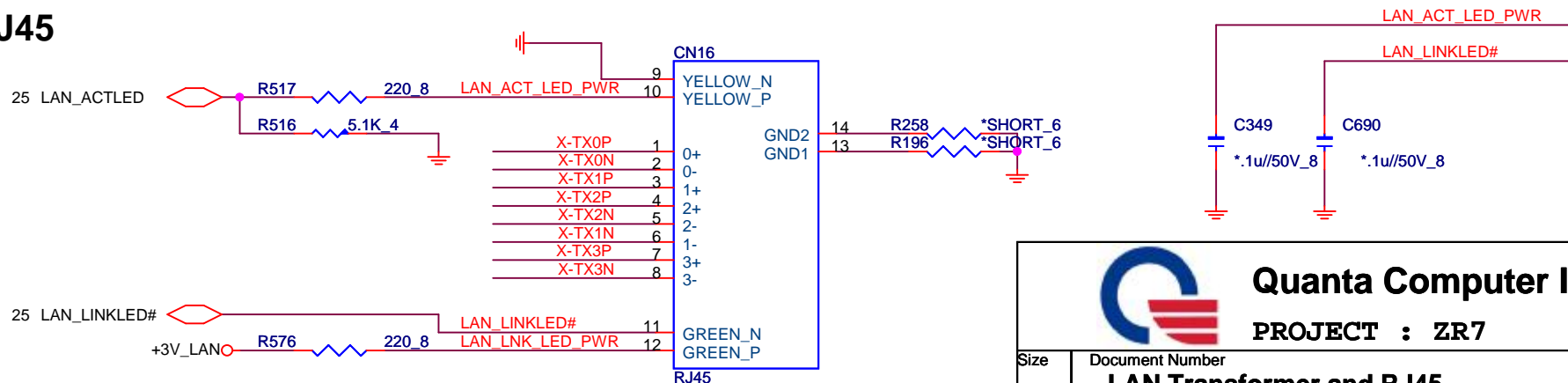
10/26 Modify

		<b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b> <b>GLAN BCM57780</b>
Size	Document Number	Rev 3B
Date: Monday, February 22, 2010	Sheet 25 of 49	

# TRANSFORMER



# RJ45



**Quanta Computer Inc.**

**PROJECT : ZR7**

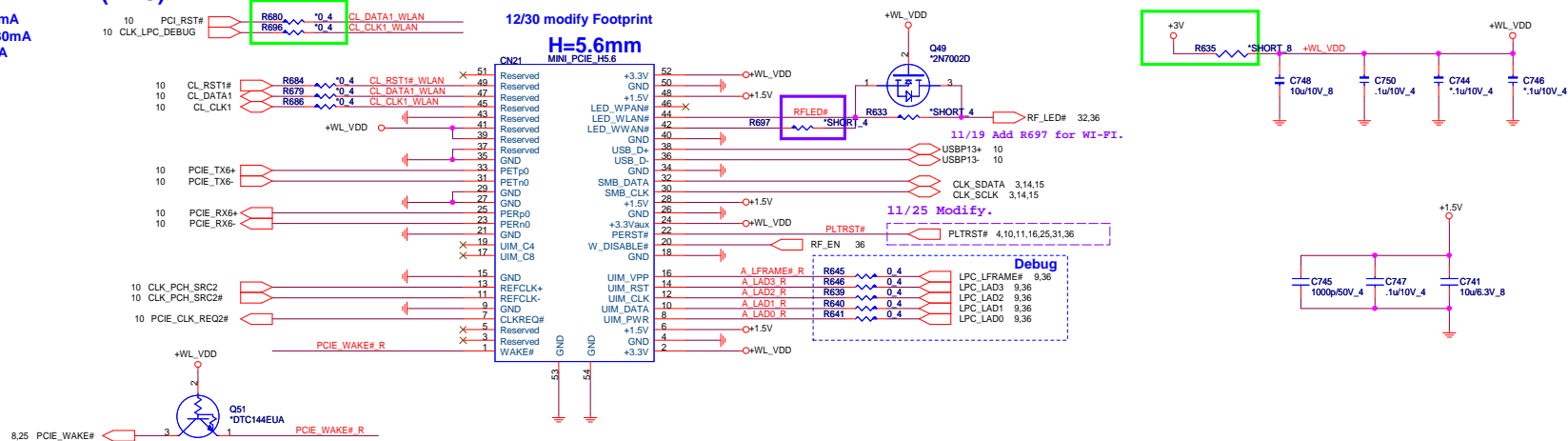
Size	Document Number	Rev
	<b>LAN Transformer and RJ45</b>	3B
Date:	Monday, February 22, 2010	Sheet 26 of 49



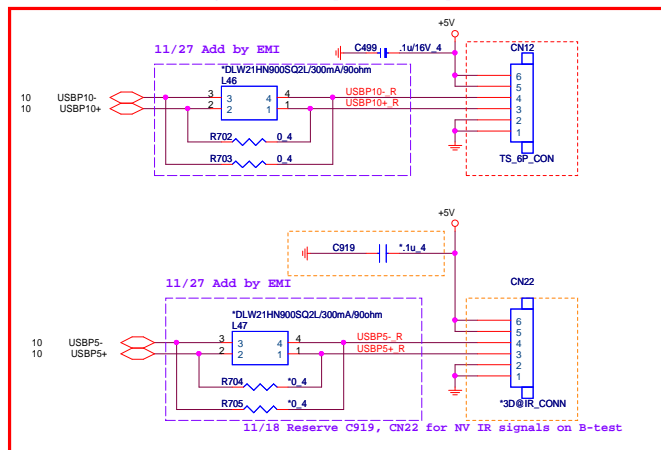
+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

12/30 modify Footprint

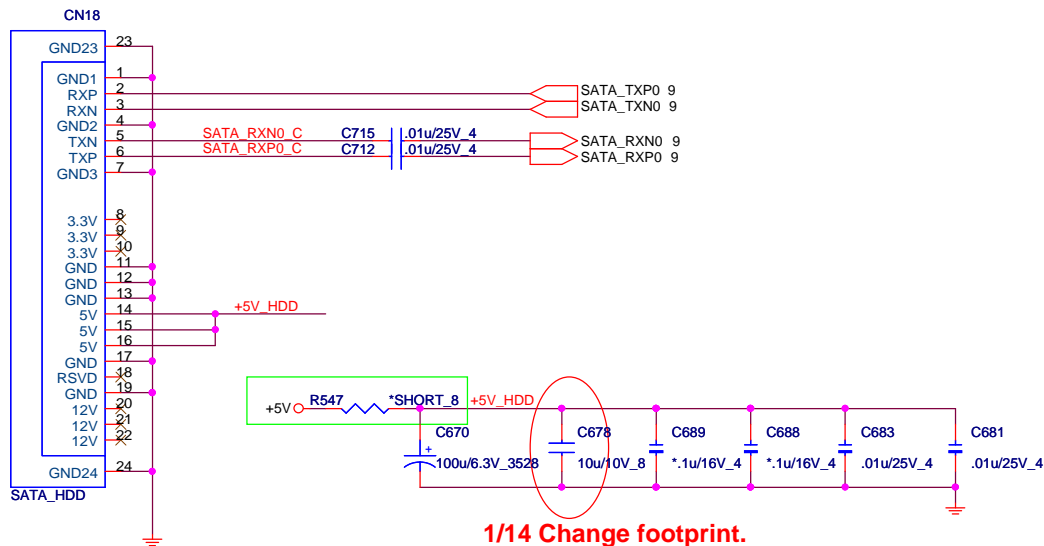
**H=5.6mm**



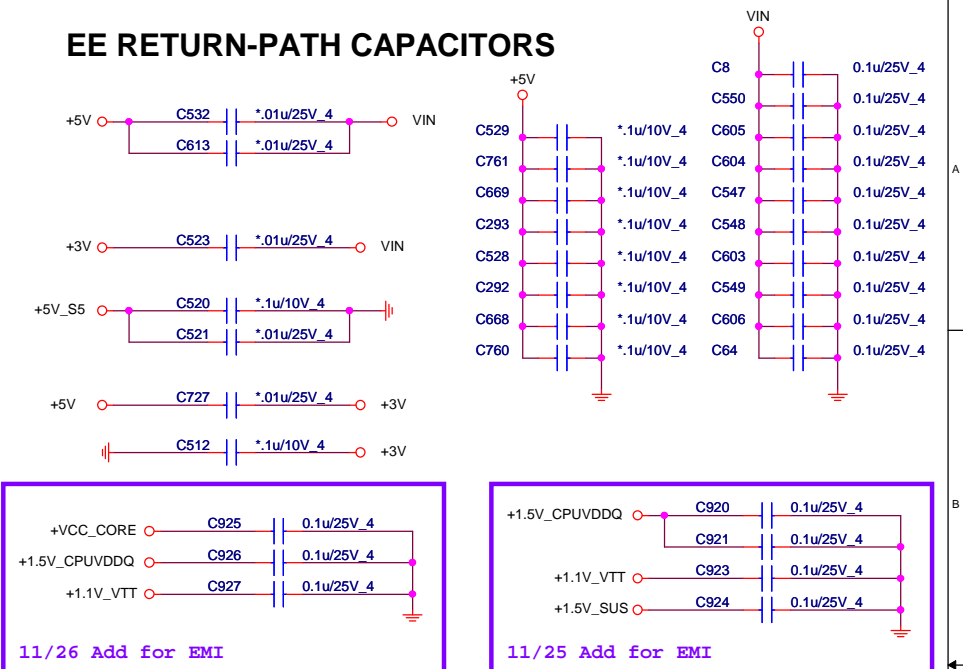
1/8 Change CN12,CN22 6pin conn footprint for Touch Screen.



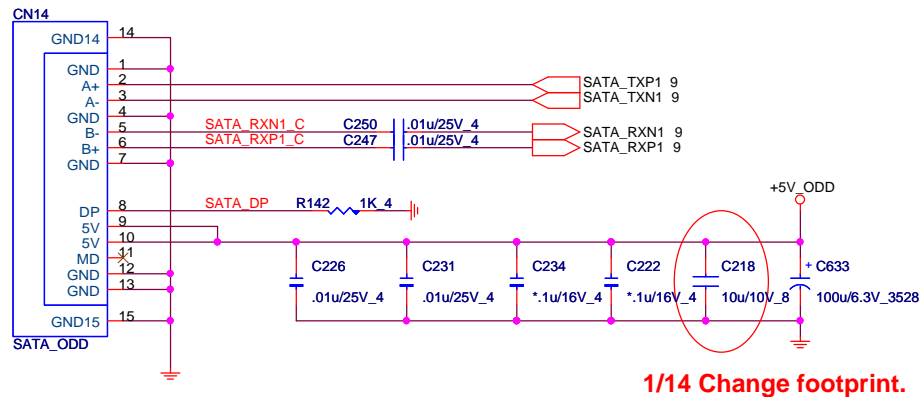
## MAIN SATA HDD



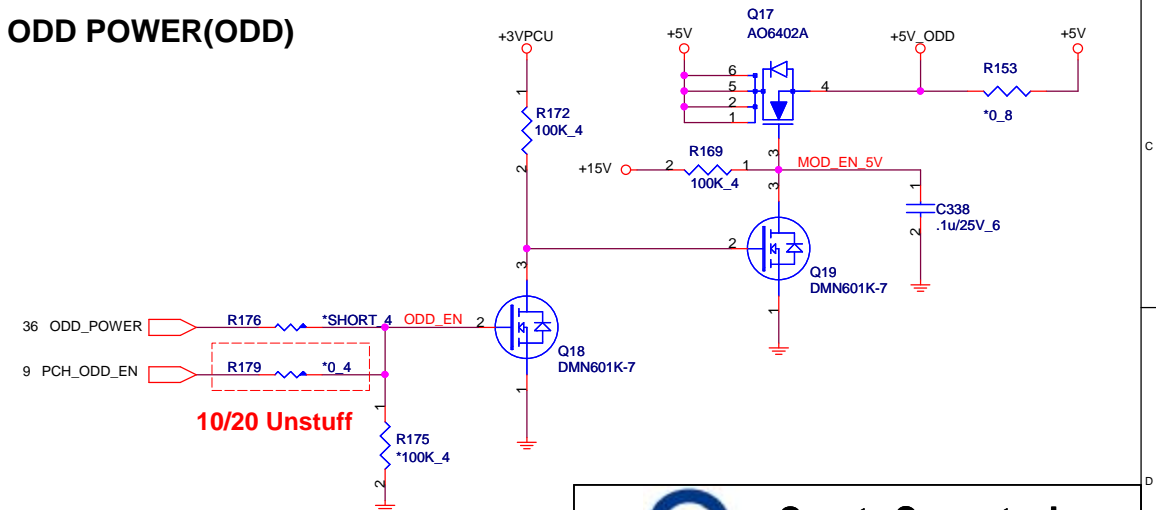
## EE RETURN-PATH CAPACITORS



## ODD (SATA)



## ODD POWER(ODD)



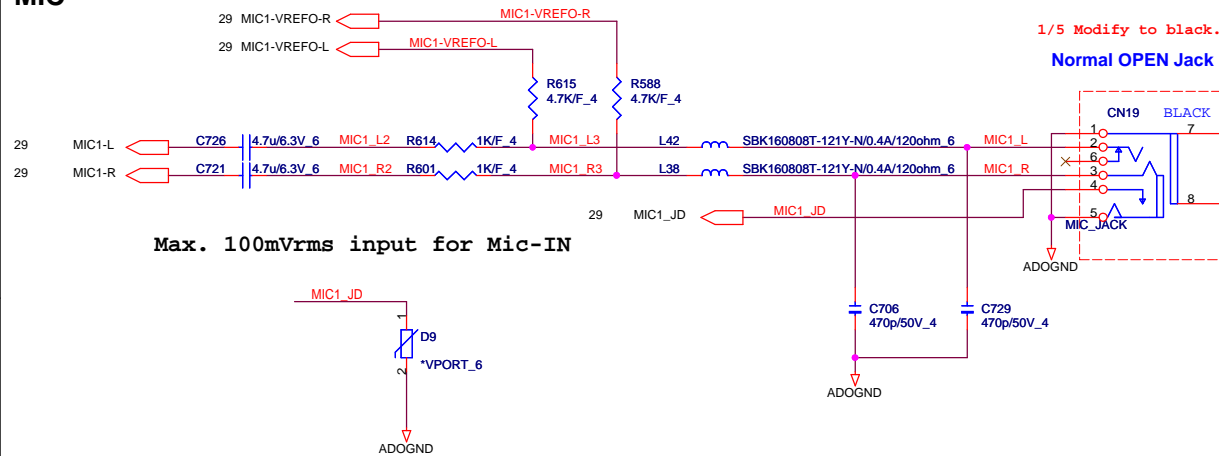
**Quanta Computer Inc.**  
PROJECT : ZR7

Size	Document Number	Rev
		3B

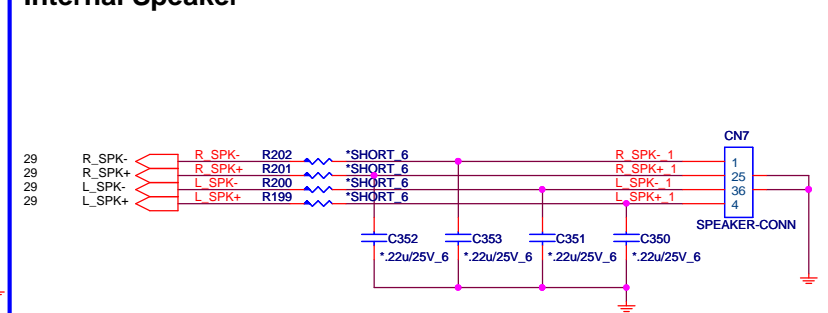
**SATA-HDD/ODD/USB-ESATA**

Date: Monday, February 22, 2010 Sheet 28 of 49

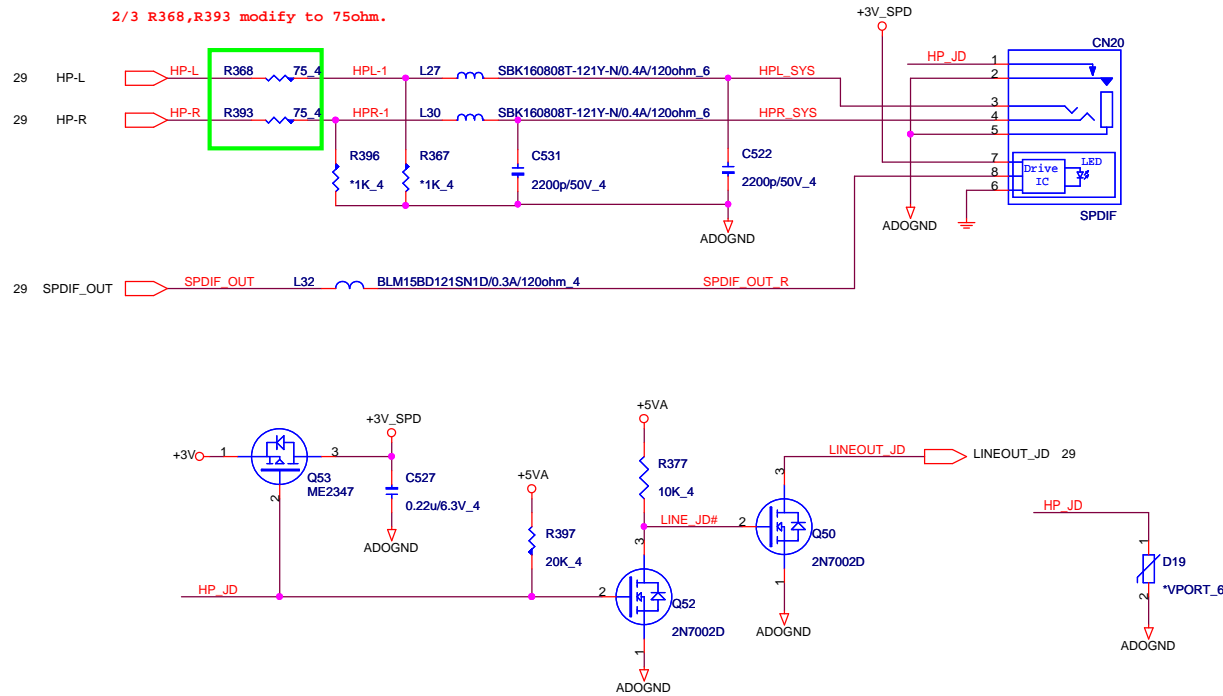



**MIC**

## Internal Speaker

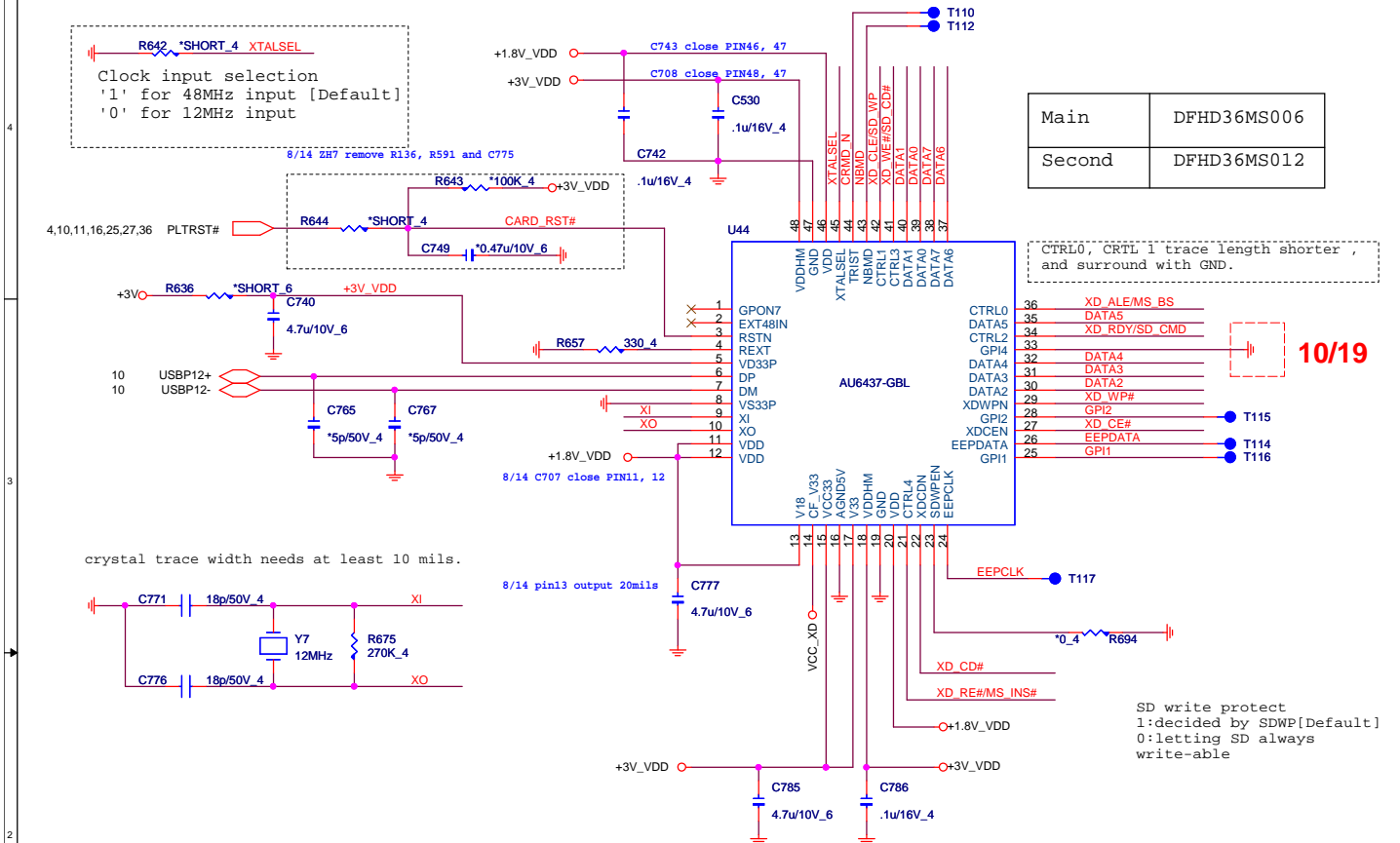


## HP/SPDIF

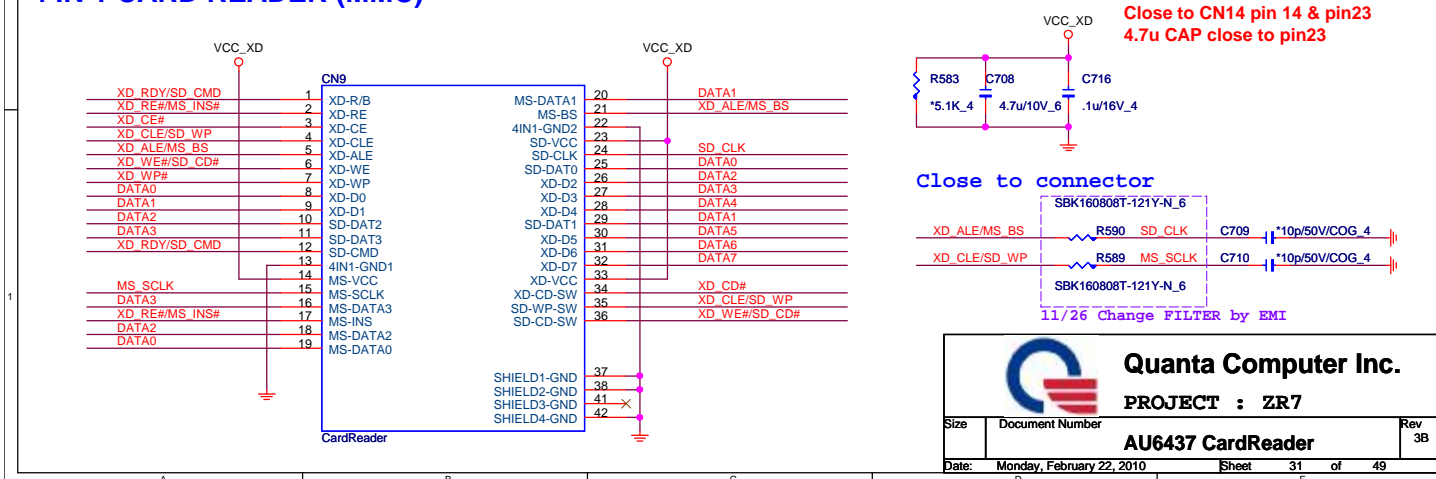


 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		
Size	Document Number	Rev
<b>AMP /AUDIO JACK CONN</b>		3B
Date:	Mondsy, February 22, 2010	Sheet 30 of 49

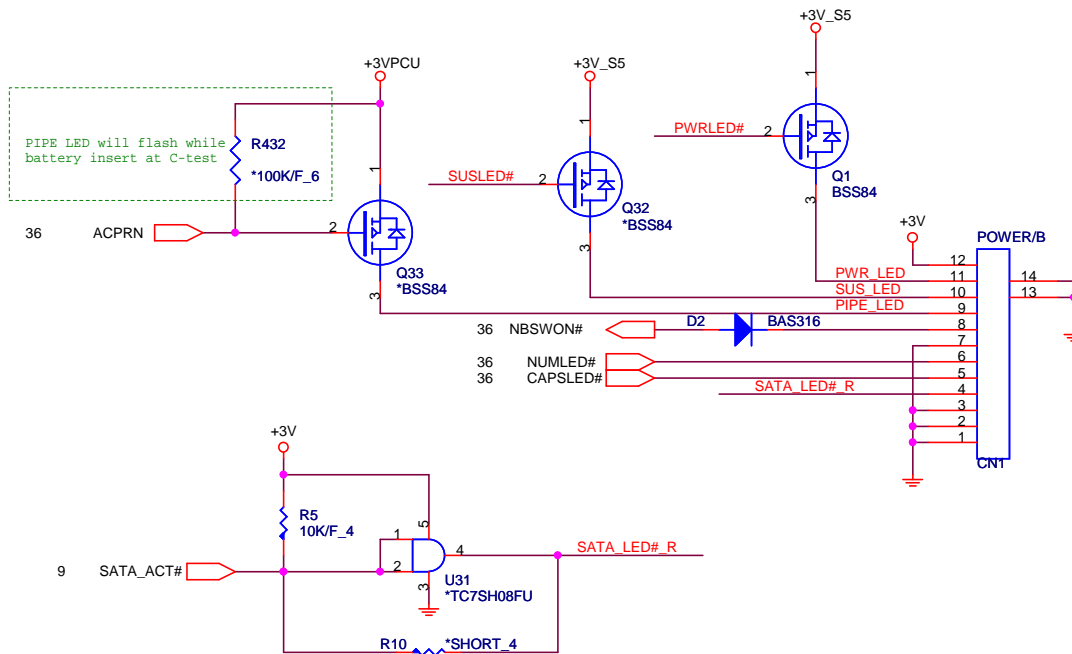
# CARD READER Controller



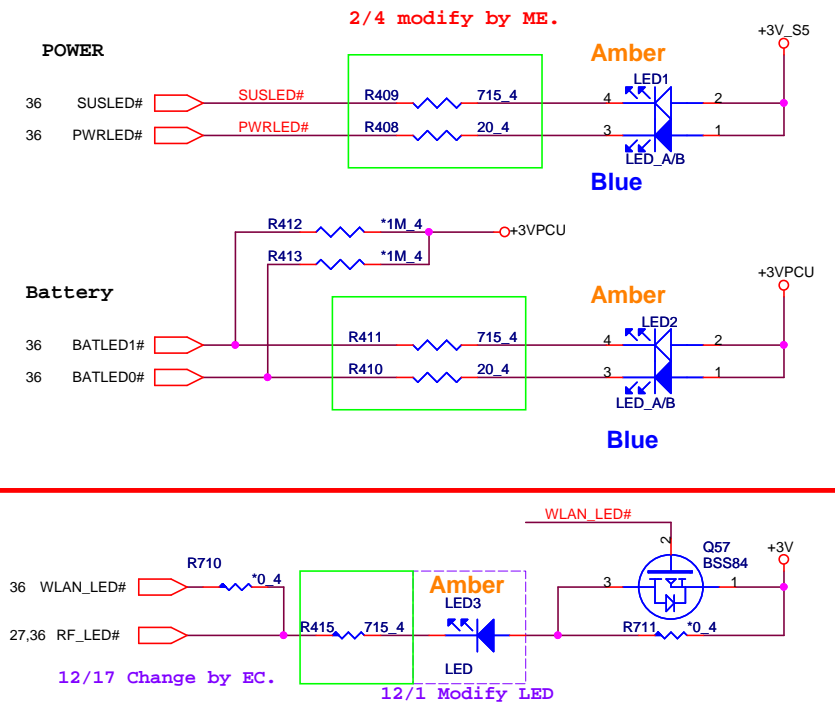
## 4 IN 1 CARD READER (MMC)



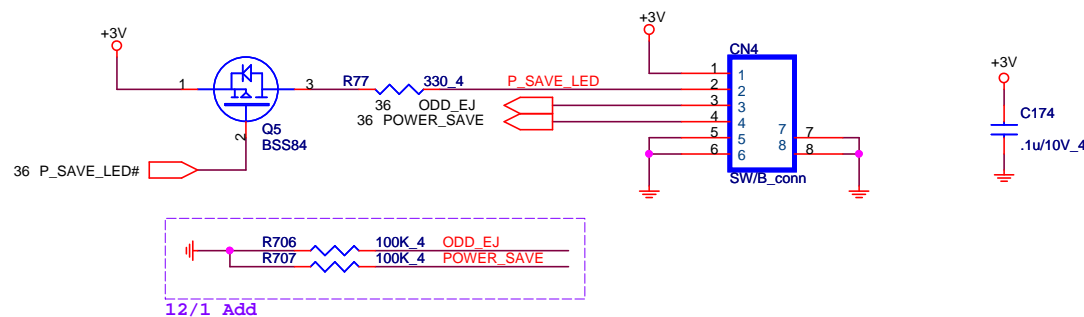
## POWER BOARD CONN(UIF)




## LED



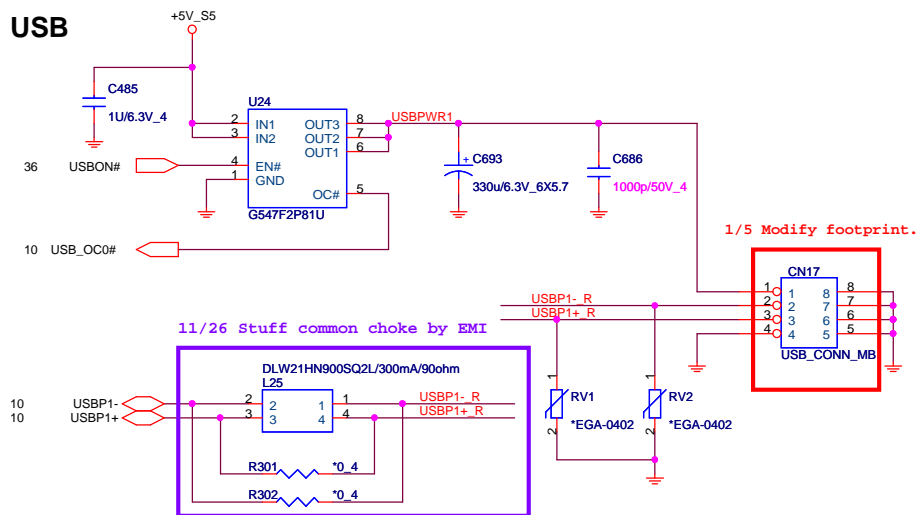
## SW /B



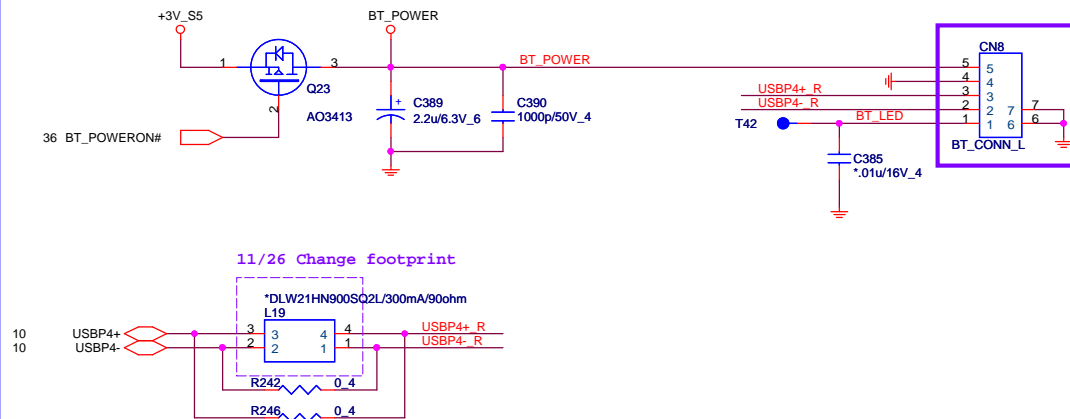
 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		
Size	Document Number	Rev 3B
<b>POWER/MMB/LAUNCH/LED</b>		
Date:	Monday, February 22, 2010	Sheet 32 of 49



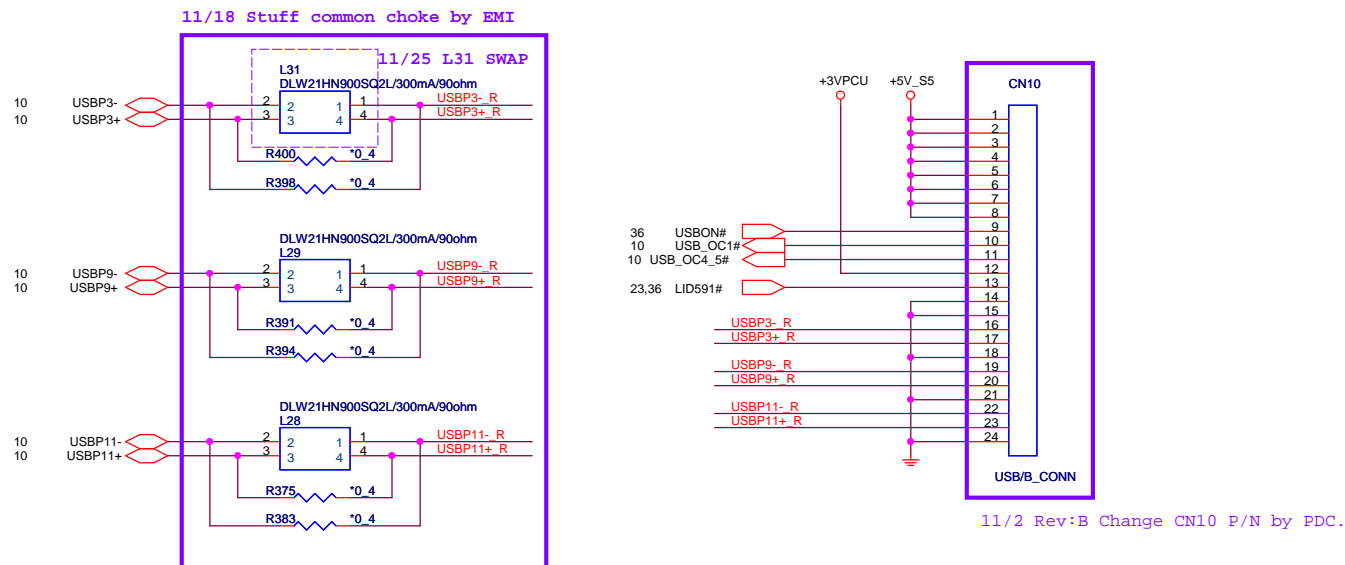
## USB




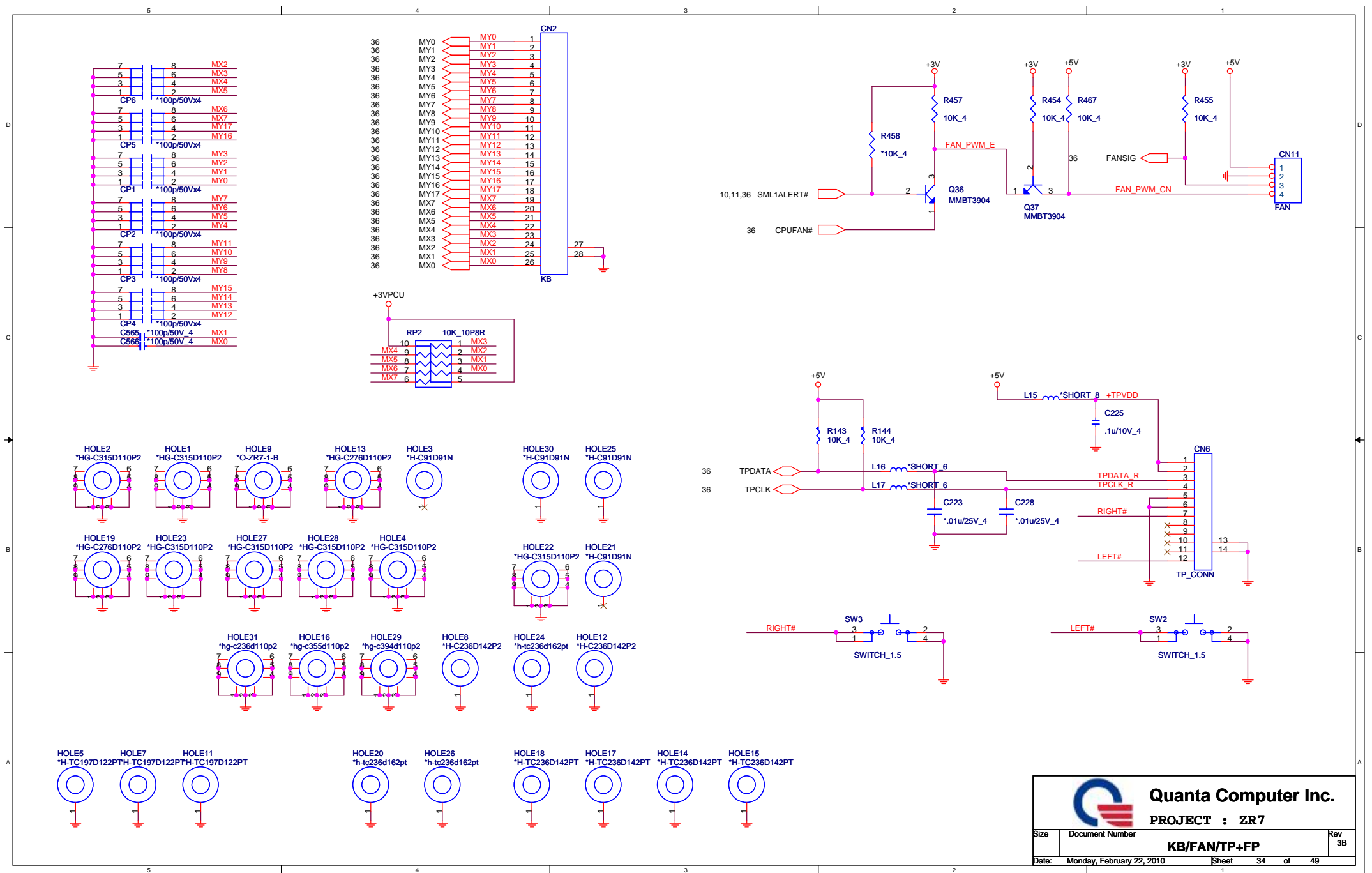
## BLUETOOTH CONNECTOR

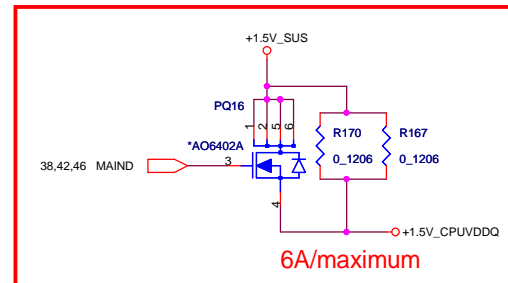
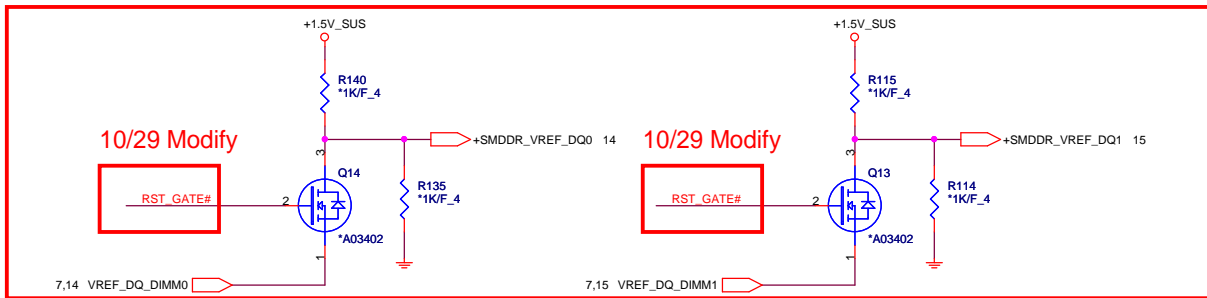
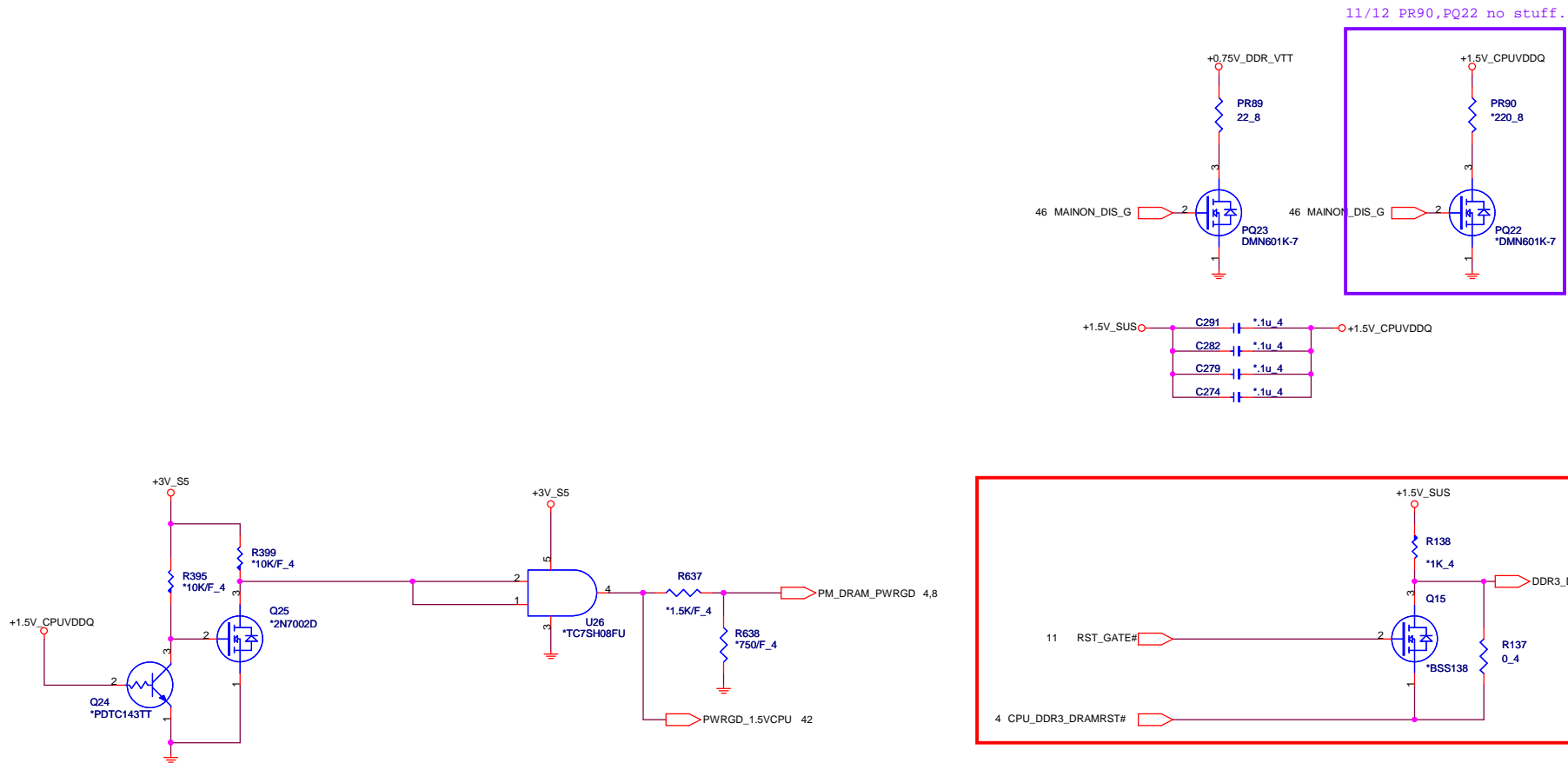


## USB/B

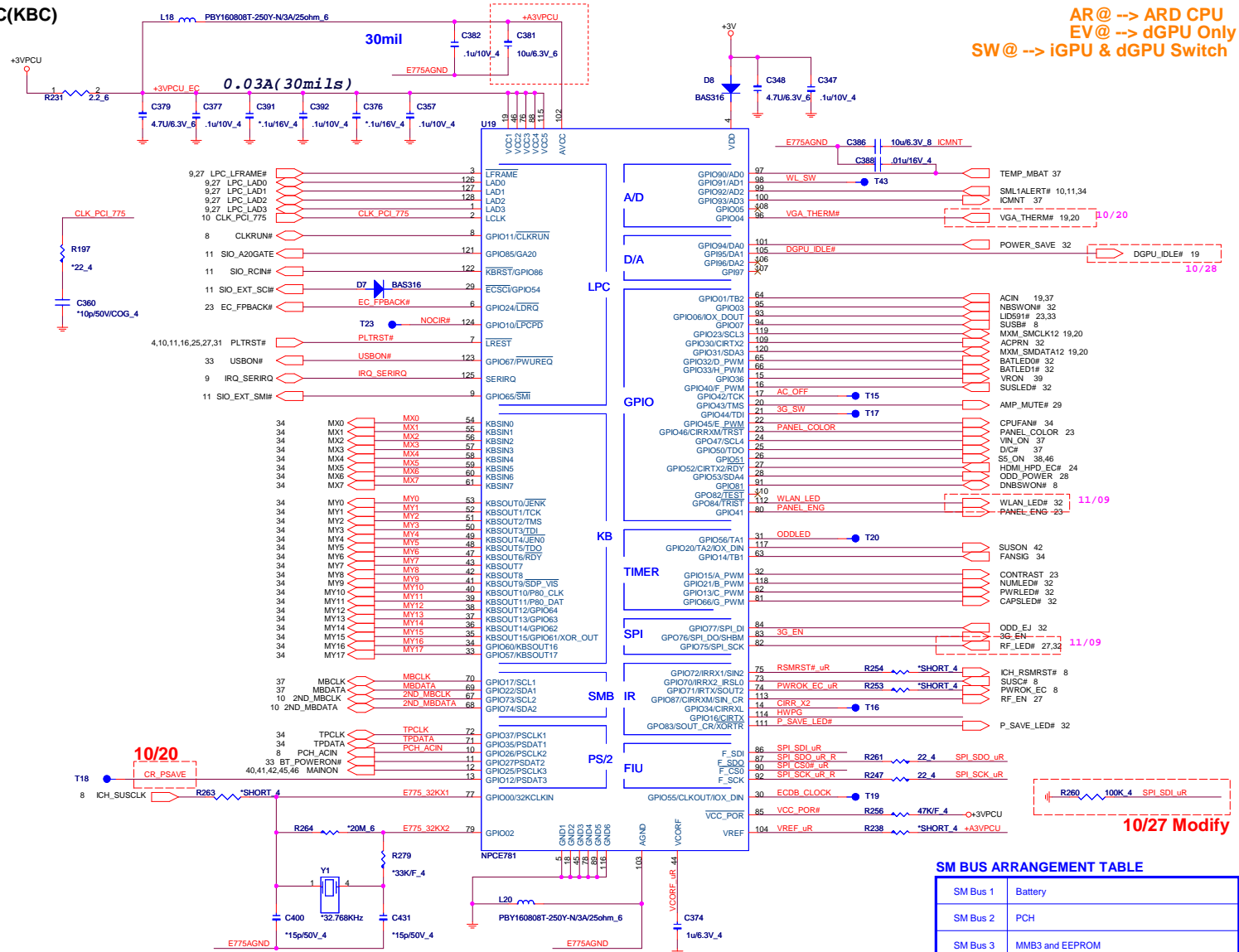


 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		Rev 3B
Size	Document Number	Date: Monday, February 22, 2010
Sheet 33 of 49		





**EC(KBC)**



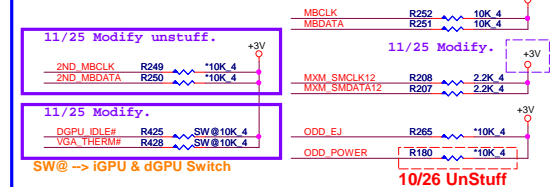
## I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

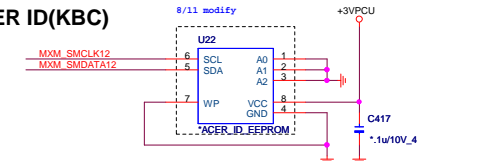
HBM — 3G EN — R255 — 10K 4 —

1/13 Confirm by vendor mail :  
Disabled (\*) if using FW device on LPC.  
Enabled (0) if using SPI flash for both system BIOS and EC firmware

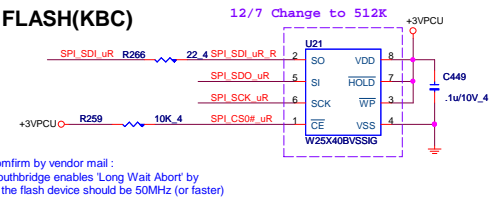
## SM BUS PU(KBC)



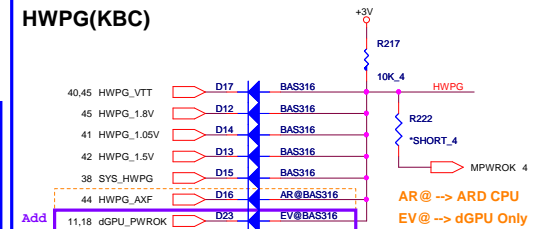
## ACER ID(KBC)



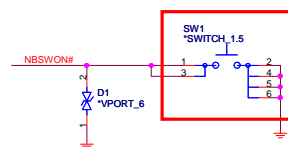
**SPI FLASH(KBC)**



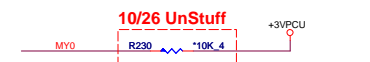
## HWPG(KBC)




## POWER-ON Switch(KBC)



### INTERNAL KEYBOARD STRIP SET(KBC)



 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		Rev 3B
Size	Document Number	
	<b>WPCE781 &amp; FLASH</b>	
Date:	Monday, February 22, 2010	Sheet 36 of 49



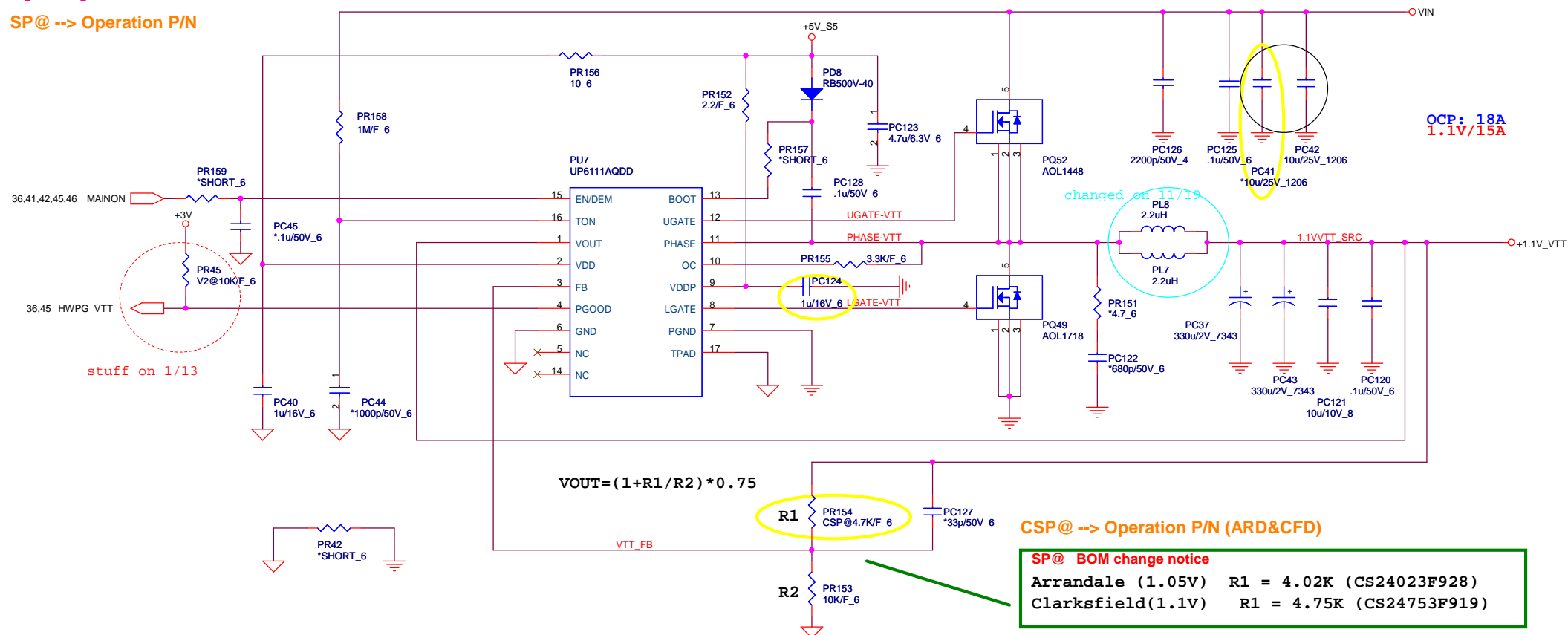






[ PWM ]

SP@ --> Operation P/N



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

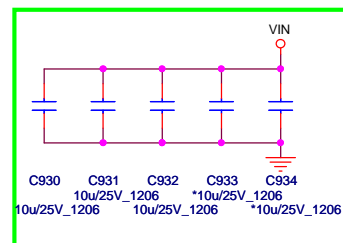
$$Frequency = 1 / (0.0036767) = 272K$$

AO1718 Rdson=3~4.3mOhm


$$L(ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.64A$$

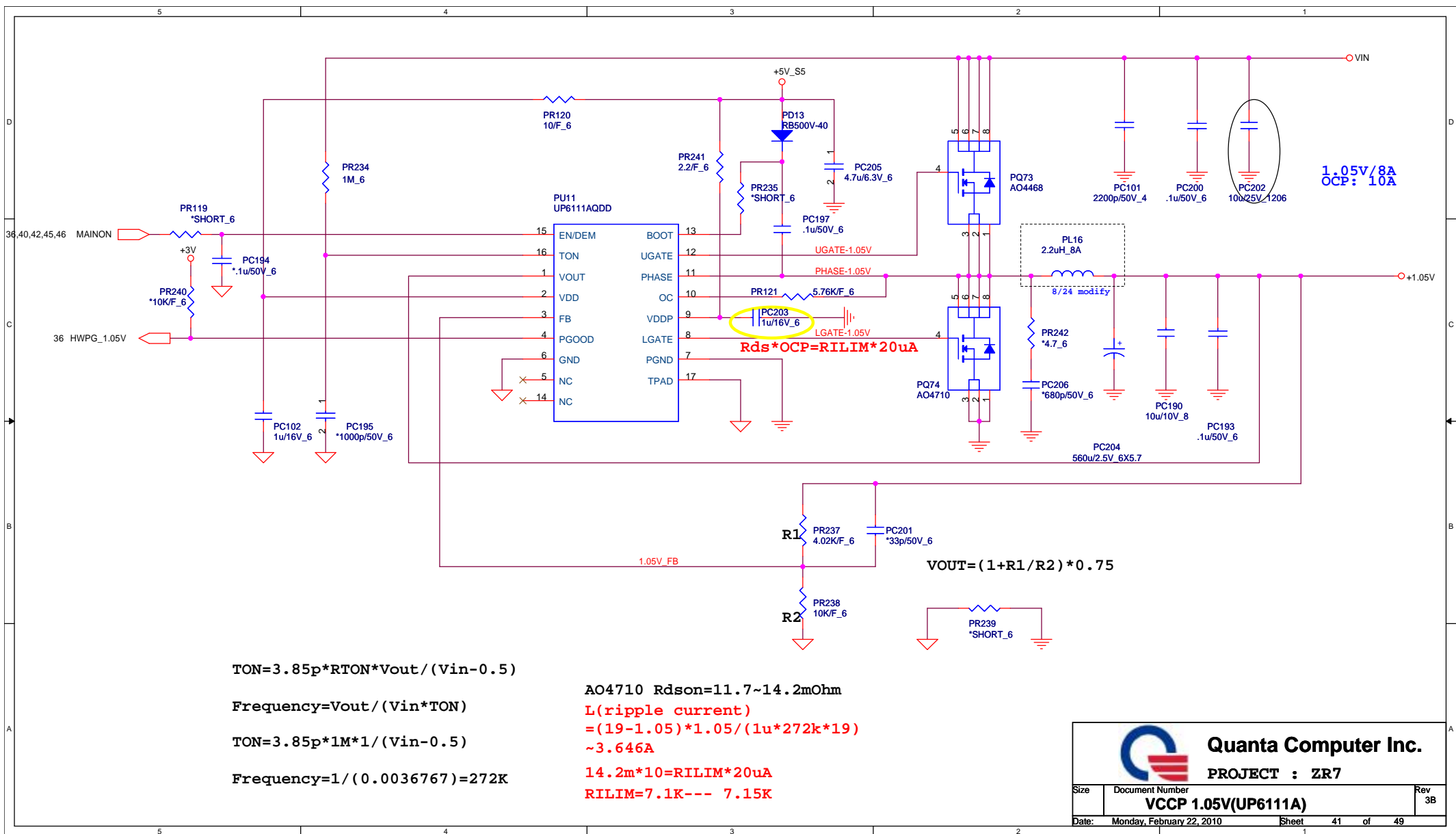
$$4.3m * 18 = RILIM * 20uA$$

$$RILIM = 3.87K \text{ --- } 3.92K$$

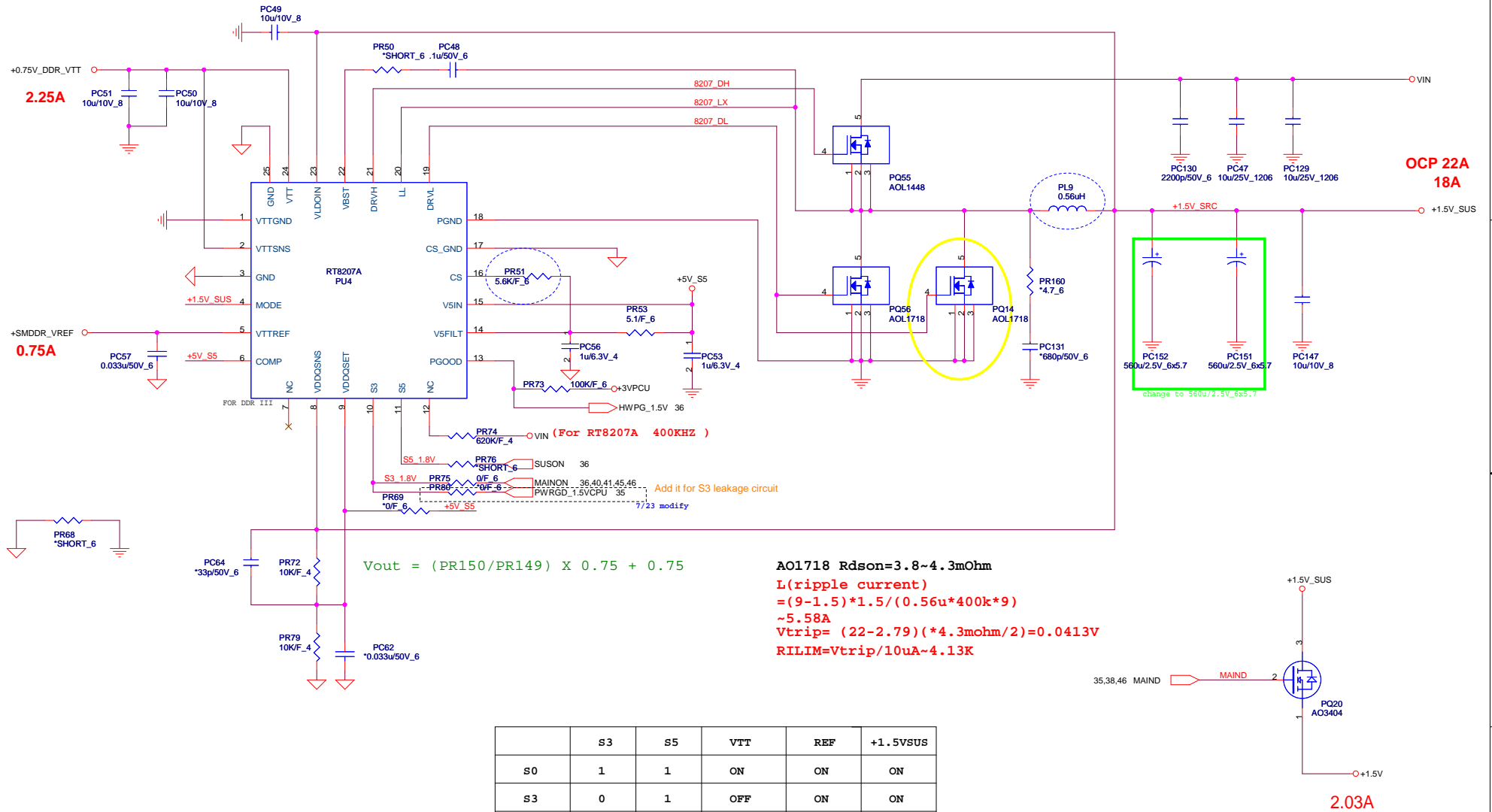


2/11 Add C930~C934 by monitor test.

 <b>Quanta Computer Inc.</b> PROJECT : ZR7		Rev 3B
Date:	Monday, February 22, 2010	Sheet 40 of 49



[PWM]



	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	OFF	ON	ON
S4/S5	0	0	OFF	OFF	OFF

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**PROJECT : ZR7**

Size Document Number  
**DDR III 1.5V(TPS51116)**

Date: Monday, February 22, 2010 Sheet 42 of 49

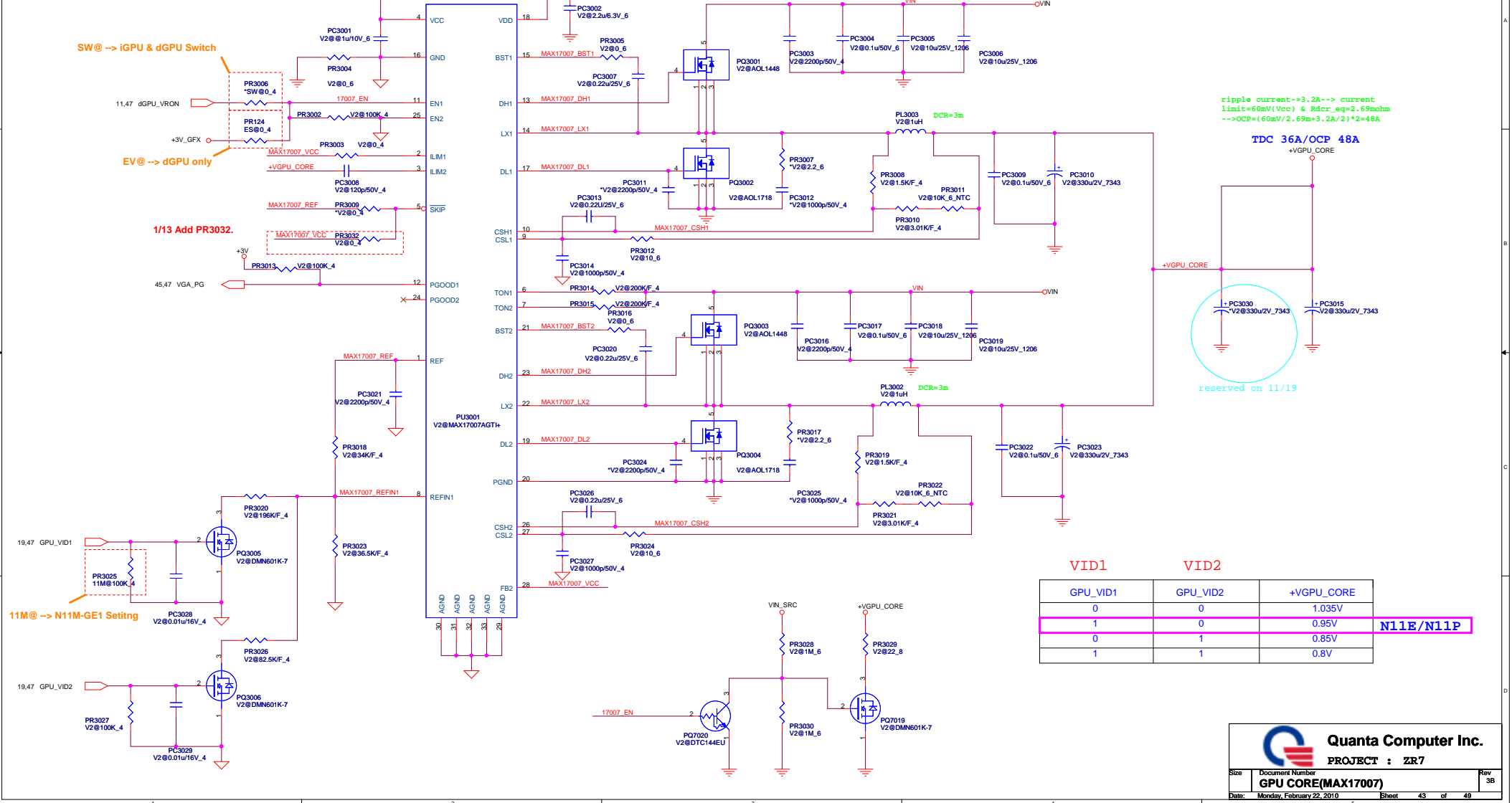
Rev 3B

11/16 Change VGPU\_CORE to two phase solution.

EV@ --&gt; External VGA SKU

**SW@ --> iGPU & dGPU Switch**

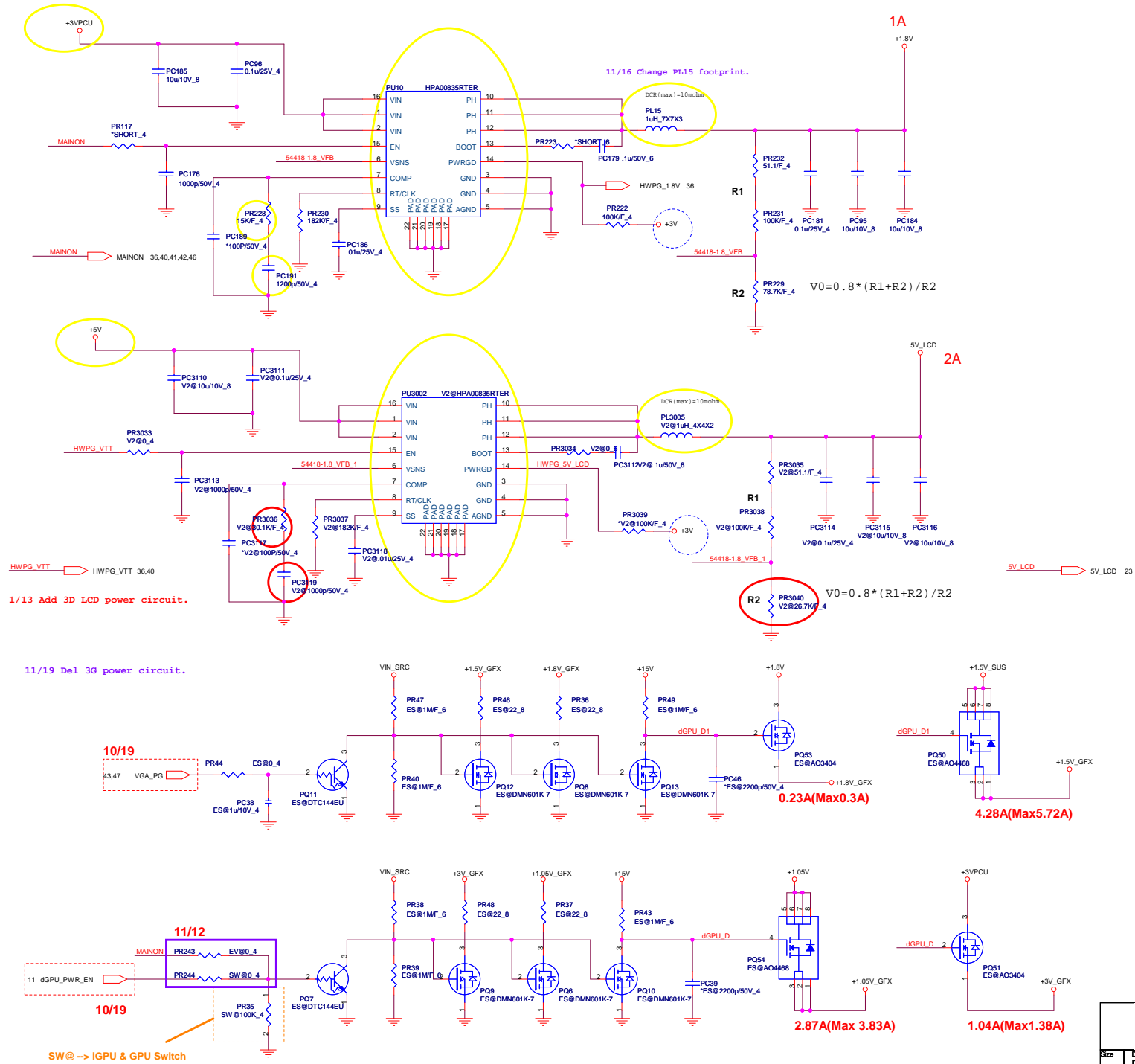
## 11M@ --> N11M-GE1 Setitng





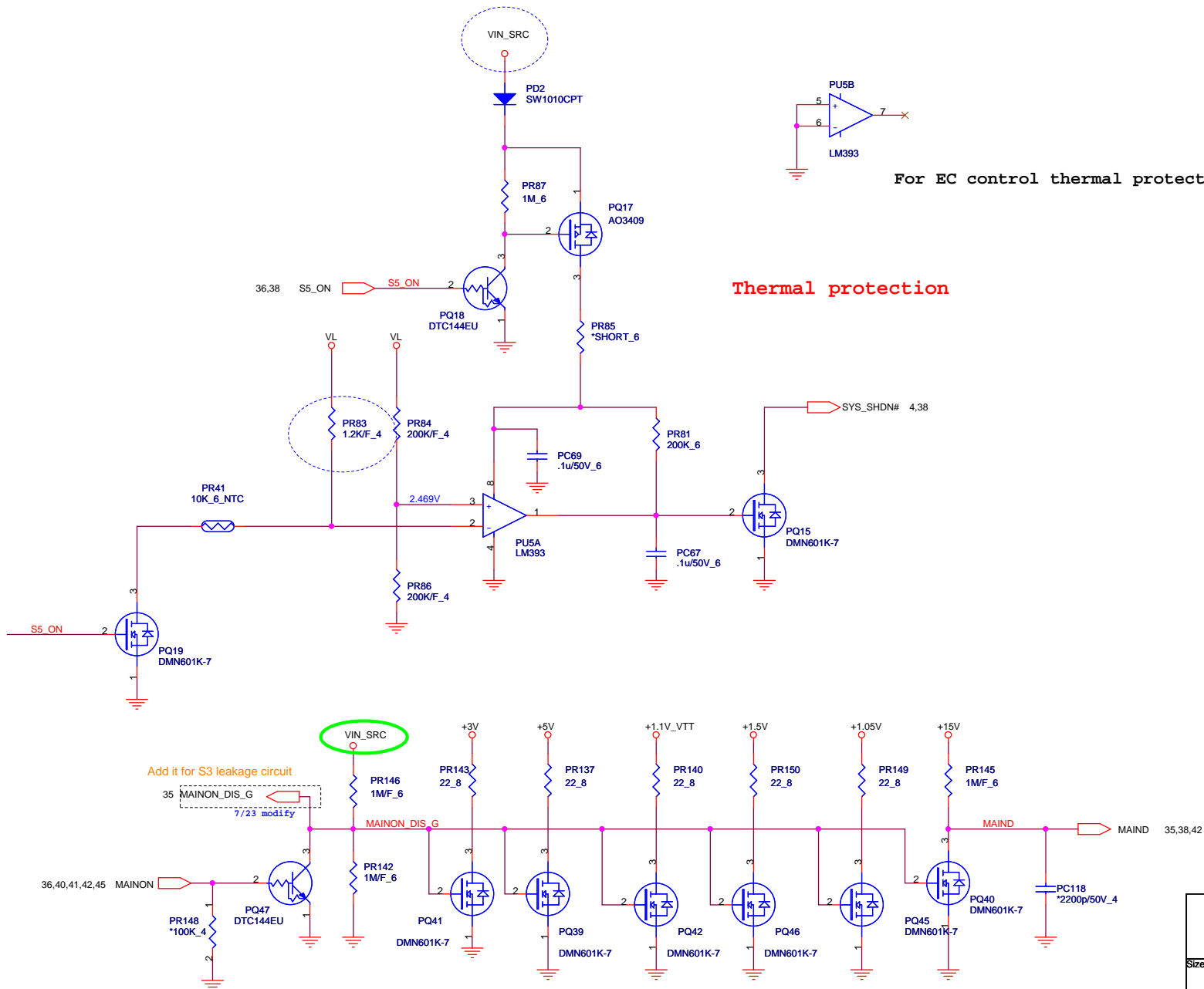



ES@ --> External VGA SKU  
SW@ --> iGPU & GPU Switch



**Quanta Computer Inc.**  
PROJECT : ZR7

Size	Document Number	Rev
	Discharge(1.8V)	38
Date	Monday, February 22, 2010	Sheet 45 of 49



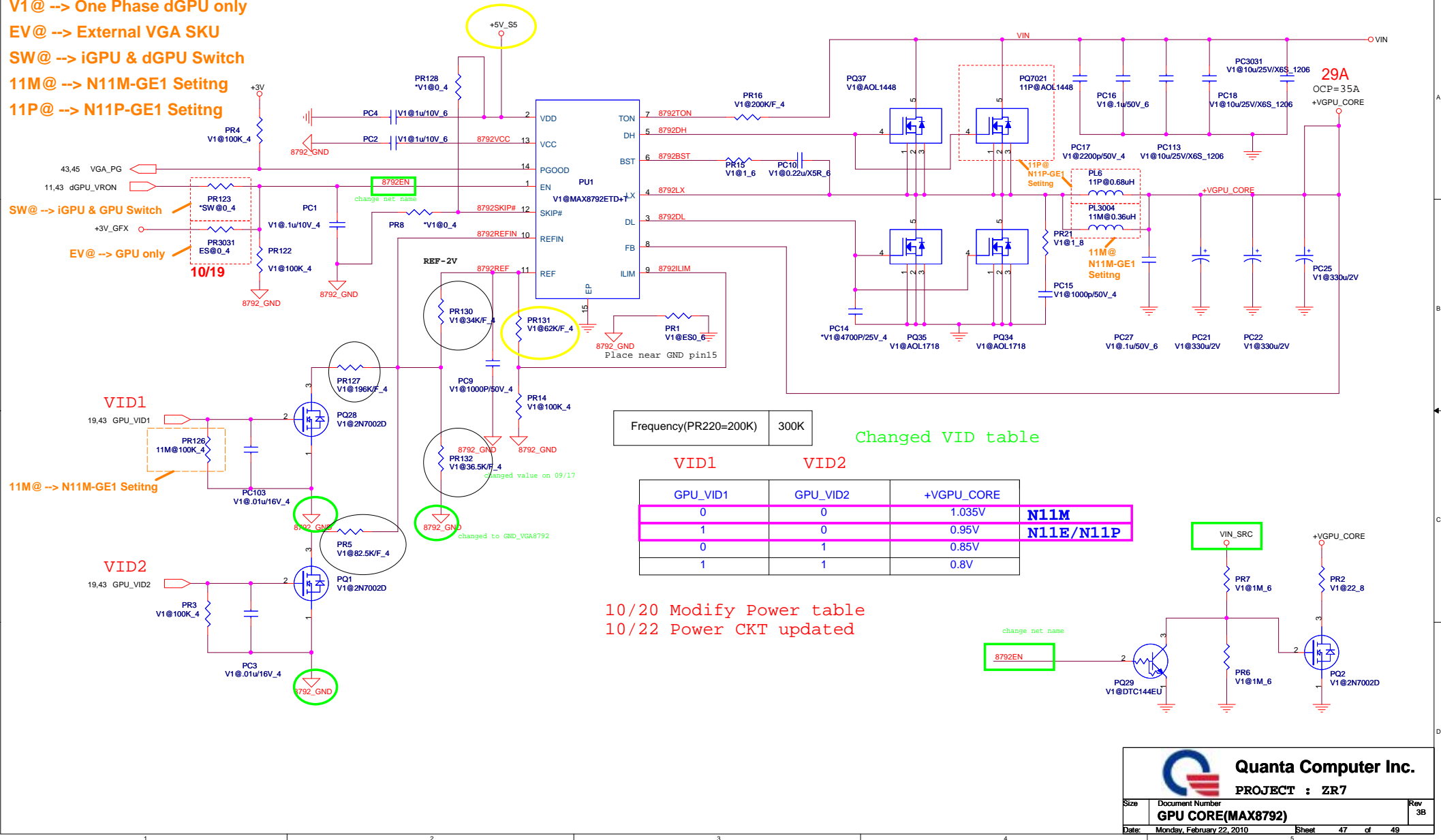
 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		
Size	Document Number	Rev
	<b>Thermal Protection</b>	3B
Date:	Monday, February 22, 2010	Sheet 46 of 49

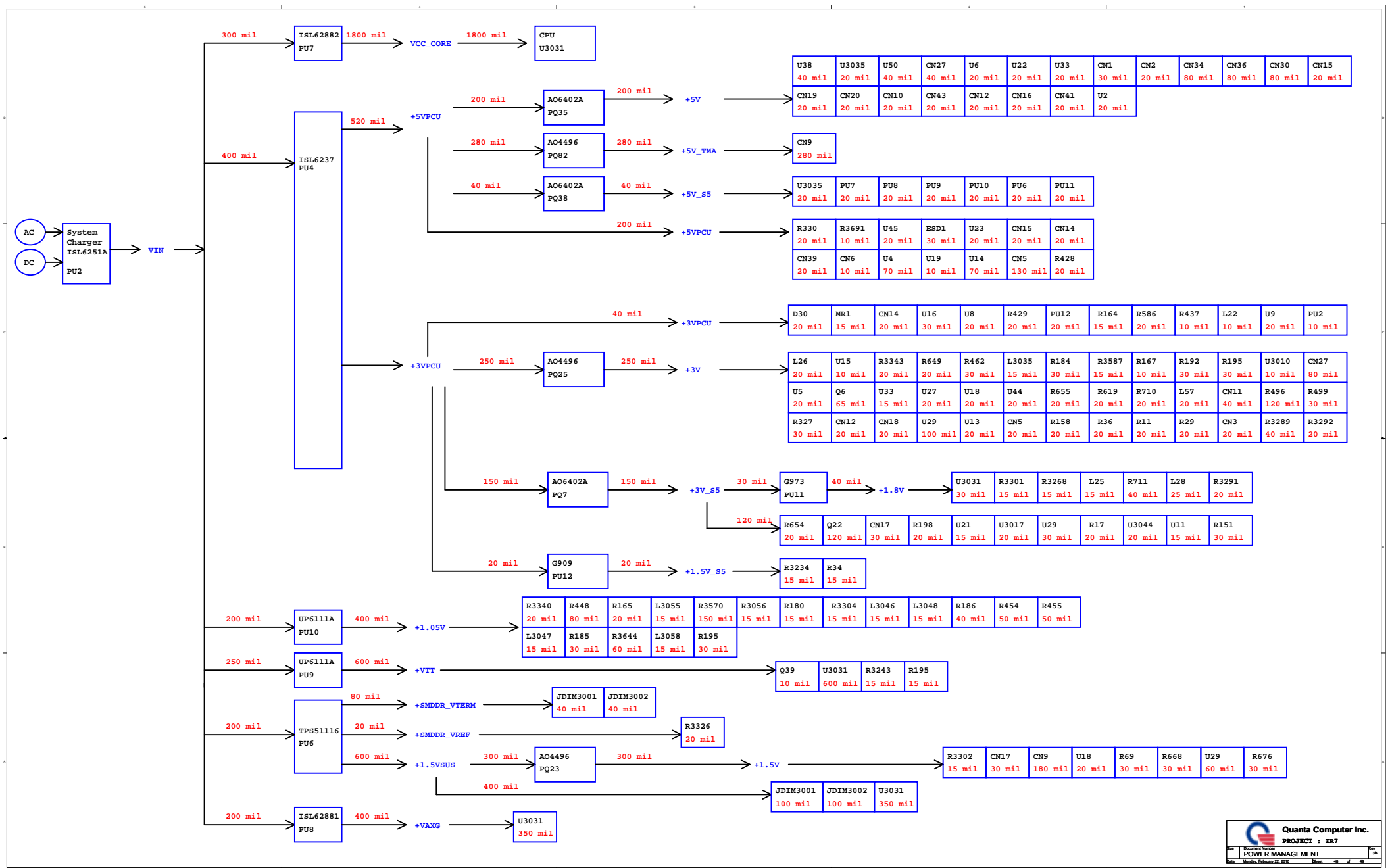
V1@ --> One Phase dGPU only  
 EV@ --> External VGA SKU  
 SW@ --> iGPU & dGPU Switch  
 11M@ --> N11M-GE1 Setitng  
 11P@ --> N11P-GE1 Setitng

SW@ --> iGPU & GPU Switch  
 EV@ --> GPU only


VID1  
 19,43 GPU\_VID1  
 11M@ --> N11M-GE1 Setitng

VID2  
 19,43 GPU\_VID2





Model	REV	CHANGE LIST	MODEL	ZR7
ZR7 MB	2A	11/2 Page33 Change CN10 P/N by POC.	FROM	To
		11/5 Page9 change R338 and R594 to 10K ohm by checklist.	1A	2A
		11/5 Page10 Add R699 connect XTAL25_IN to Gnd on EV sku and stuff Xtal components by checklist.	1A	2A
		11/5 Page11 un-stuff R318 and del C459 and add R698 contact VCCLAN to GND by checklist.	1A	2A
		11/9 Page32 change W/L LMD signal to control by EC.	1A	2A
		11/9 Page34 Add EC pin82/112 for W/L LMD control by EC.	1A	2A
		11/12 Page35 PR90,PQ22 no stuff.	1A	2A
		11/12 Page45 Add PR243,PR244 for option.	1A	2A
		11/16 Page23 CMS Add LVDS signal to two channel and change CN3 to 8pin conn.	1A	2A
		11/16 Page43 GPU VCCHE power change to two phase solution.	1A	2A
		11/16 Page27 Add CN12 8pin conn for Touch Screen by ME.	1A	2A
		11/16 Page44 Change P04 footprint by SMT.	1A	2A
		11/16 Page45 Change FL15 footprint to CHOKER-PCMC063T-3R3MM-NB4 by SMT.	1A	2A
		11/16 Page39 Change P08 footprint to qfn40-5x5-4-41p-0.75h-smt by SMT.	1A	2A
		11/16 Page37 Change P03 footprint to QFN40-5X5-5-33P-SMT by SMT.	1A	2A
		11/18 Page10 Delete R597, C444,C445 for cancel 3G function.	1A	2A
		11/18 Page10 R368,R393 modify from 470m to 510m by Realtek.	1A	2A
		11/18 Page10 Change BOARD_ID0-2 to BOARD_ID1-3.	1A	2A
		11/18 Page11 Change GP107 to BOARD_ID0 and reserve R439 PD.	1A	2A
		11/18 Page36 Add D23 to connect to dGPU_PWRON on EV sku.	1A	2A
		11/18 Page9 Change P/N follow ZR7B that use right angle connector.	1A	2A
		11/18 Page27 Reserve C919, CN22 for MV IR signals on B-test.	1A	2A
		11/19 Page1 Change U19 PM to AL203197082 by vendor.	1A	2A
		11/19 Page11 Change CN9 footprint & P/N follow ZR7B.	1A	2A
		11/19 Page27 Add R697 for MT-FI.	1A	2A
		11/19 Page11 Add R442, R440 to dGPU_PWRON_R and stuff R321 on EV sku.	1A	2A
		11/19 Page23 Modify CMS pin define.	1A	2A
		11/20 Page43 Add PR124 on EV sku.	1A	2A
		11/20 Page14 Change core logic cap .1uF CH410032R35 to CH4102K1B03 by SMT.	1A	2A
		11/20 Page43 del 3G power circuit.	1A	2A
		11/20 Page14 del HOLE10,Add HOLE5,HOLE6,HOLE7,HOLE8,HOLE11,HOLE12,HOLE14,HOLE15,HOLE17,HOLE18,HOLE20,HOLE24,HOLE25,HOLE26,HOLE30 P/N	1A	2A
		11/25 Page10 Q26,Q29 change to unstuff , Add R700,R701 0 ohm for S1 leakage	1A	2A
		11/25 Page20 CL51 change to OCT343 package	1A	2A
		11/25 Page14 Change HOLE8,HOLE12 footprint to M-C216D142P2 , Change HOLE5,HOLE7,HOLE11 footprint to M-TC19V1D122PT , Change HOLE14,HOLE15,HOLE17,HOLE18 footprint to M-C216D142PT , Change HOLE20,HOLE24,HOLE26 footprint to M-TC16D162PT , Change HOLE9 footprint to O-SMT-1-8	1A	2A
		11/25 Page36 R428 change to dGPU_IDLE# signal and value to SW SKU , R428 change value to SW SKU , R249,R250 change to unstuff	1A	2A
		11/25 Page28 Add C920,C921,C923,C924 0.1uF for EMI	1A	2A
		11/25 Page33 L31 SWAP for Layout House	1A	2A
		11/25 Page27 Modify LTR878_7726 net name to PLTR878	1A	2A
		11/26 Page33 Change L19/L25 footprint , Stuff L25 common choke & unstuff R301,R302 by EMI	1A	2A
		11/26 Page23 Change L2 footprint	1A	2A
		11/26 Page23 Change R598,R599 to PLTR for EMI	1A	2A
		11/26 Page28 Add C925,C926,C927 for EMI	1A	2A
		11/26 Page11 Modify R422 Value to 1V0 SKU	1A	2A
		11/27 Page11 del R440	1A	2A
		11/27 Page20 CH1,CL05 change CO9603 package	1A	2A
		11/27 Page16 CH4,CL09 change CO9603 package	1A	2A
		11/27 Page23 Add CH5 pin45 to GND	1A	2A
		11/27 Page27 Add L46,L47,R702,R703,R704,R705 by EMI	1A	2A
		11/27 Page10 Modify C699,C703 to 27pF	1A	2A
		11/27 Page18 Modify C691,C690 to 27pF	1A	2A
		12/1 Page27 Modify CN13 to 6 pin connector	1A	2A
		12/1 Page32 Modify LMD3 & Add R706,R707 PD by EC CDD_RV & POWER_SAVE	1A	2A
		12/1 Page9 Add R708,R709 by SPI ROM	1A	2A
		12/18 Page22 Add R710,R711,Q57 by EC.	2A	3A
		12/18 Page23 Add R712,R713 by 3D feature.	2A	3A
		12/18 Page47 Change PL6 footprint to choke-spl1136-2r2-smt by SMT.	2A	3A
		12/29 Page27 Change CN21 footprint to MIPCI-800055P8052GX00p1-52P-smt by SMT.	2A	3A
		12/29 Page23 Add F1 by safety.	2A	3A
		12/29 Page24 Change Q16, Q19 P/N & add F2 by RNDI submit and safety; del U15, U16, U18.	2A	3A
		12/29 Page10 Change CN19 color to black P/N: OPT08PR110 by ACM.	2A	3A
		1/5 Page33 Change CN17 footprint to USB-UN1120C-RARED-7P-4P-8-V-SMT by POC.	2A	3A
		1/7 Page23 Change Q12 of dGPU_select# signal design by leakage issue.	2A	3A
		1/7 Page9 Change BT1 P/N to DFHD02M8784 by ME issue.	2A	3A
		1/8 Page27 Change CN12,CN22 8pin conn footprint for Touch Screen and IR.	2A	3A
		1/11 Page23 Add L48 & stuff L2 and un-stuff R28 and R29 by EMI.	2A	3A
		1/13 Page24 Add C928 by EMI.	2A	3A
		1/13 Page10,36 Change C711,C182 to 10U 6.3V.	2A	3A
		1/14 Page23 Change LVDS connector Pin# define from NC to LCDVCC & add J3 by 3D PWR.	2A	3A
		1/14 Page28 Change C218,C678 to 10U/10V_8 and footprint 0805.	2A	3A
		2/3 Page 16-22 Change U33 footprint to fcbga973-nvidia-nlp-ae-al by NV.	2A	3A
		2/3 Page 30 Change R368,R393 to 75ohm.	3A	3B
		Power modify:	1A	2A
		11/19 Take out JP12, JP9, JP5, JP6, JP7, JP19, JP20, JP8, JP10, JP11,JP13, JP15, JP16, JP1, JP17, JP14, JP18.	1A	2A
		11/19 Page38 Change PC198 value; change PR114 from 191K to 182K, PR115 from 220K to 200K,PR106 from 100K to 1K,PR105 from 200K to 150K.	1A	2A
		11/19 Page40 Change PL7,PL8 from 1.0uH to 2.2uH.	1A	2A
		11/19 Page39 Change FL10,PL11 from DC-36T0M000 to CV-18V0M024.	1A	2A
		11/19 Page43 Reserve PC3030.	1A	2A
		11/23 Page37 PR19 change to 150K , PR20 change to 39K , PC112 change to 1U 25V	1A	2A
		12/29 Page47 Change PL7,PL8,PL15,PL16 footprint to CHOKER-PCMC063T-3R3MM-SMT by SMT.	2A	3A
		12/29 Page37 Change PR136 footprint to RC3720-SMT by SMT.	2A	3A
		1/5 Page37-48 Change Footprint from CHOKER-ETQ4LR36WPC to CHOKER-ETQ4LR36WPC-SMT by POC.	2A	3A
		1/11 Page37 Add PC3100-PC3109 by EMI.	2A	3A
		1/11 Page47 Change value of PQ7021,PL6,PL3004 by ROM.	2A	3A
		1/13 Page43 Reserve PR3032 by PWR.	2A	3A
		1/13 Page45 Reserve circuit of LCDVCC by PWR.	2A	3A
		2/10 Page37 Reserve ECL-BCS by EMI.	3A	3B
		2/11 Page38 Del PD3 by power.	3A	3B
		2/11 Page40 Add C930-C934 by monitor test.	3A	3B

 <b>Quanta Computer Inc.</b> PROJECT : ZR7		DOC NO.	PROJECT MODEL :	ZR7	APPROVED BY:		DATE:	2009/11/06
Change list2 <small>Rev 28</small>			PART NUMBER:		DRAWING BY:		REVISION:	1A